Maximum Likelihood Sequence Estimation for Chromatic Dispersion and Polarization Mode Dispersion Compensation in 3-Chip DPSK Modulation Format

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Abstract: We show that maximum-likelihood-sequence estimation (MLSE) of 10-Gbit/s 3-chip DPSK exhibits 1.6 dB penalty bound for 100-ps DGD and the CD tolerance 1.5 times of that of MLSE-equalized 10-Gbit/s 2-chip DPSK. © 2007 Optical Society of America

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1. Introduction

Differential phase-shift keying (DPSK) has been widely employed in long-haul high-speed optical transmission applications because it offers better tolerance to fiber nonlinear effects and shows 3-dB OSNR sensitivity improvement when balanced detection is employed. As a promising method to improve the performance of the DPSK signal, multi-chip DPSK (MC-DPSK) detection was recently proposed [1]. By using this detection technique, the performance of the DPSK signal can approach that of coherent-detected PSK with the increase of chip number. The least complex MC-DPSK scheme is 3-chip DPSK which requires two delay interferometers (DIs) and a 3×4 weighting matrix. In addition to the back-to-back sensitivity improvement, 3-chip DPSK also shows higher tolerance to chromatic dispersion (CD) than conventional 2-chip DPSK when a suitable weight factor is used [2]. However, such improvement is not prominent. For example, only 0.8-dB penalty reduction was exhibited for 3-chip DPSK after 100-km single-mode fiber (SMF) transmission under optimal weight factor [2].

Electrical equalizer is another promising technique for CD compensation because of its cost effectiveness and adaptive equalization ability. It is also capable of compensating polarization-mode dispersion (PMD) [3]. Maximum likelihood sequence estimation (MLSE) of conventional 2-chip DPSK for CD and PMD compensation has been investigated in [4] and [5], respectively. However, the performance improvement by MLSE in 2-chip DPSK format for CD compensation is limited by the phase-to-noise conversion [5]. In this paper, we propose MLSE in 3-chip DPSK detection and show that such method significantly outperforms pure 3-chip DPSK and MLSE-equalized 2-chip DPSK in CD and PMD compensation. Simulations show that the CD tolerance of MLSE-equalized 10-Gbit/s 3-chip DPSK is enhanced to 1.5 times of that of MLSE-equalized 10-Gbit/s 2-chip DPSK while the penalty for 100-ps differential group delay (DGD) is upper-bounded by 1.6 dB.

2. Simulation Setup



Figure 1: Simulation setup

OMG3.pdf

Fig. 1 shows the simulation setup. 10-Gbit/s DPSK signal is obtained by feeding a continuous-wave light into a dual-driven Mach-Zehnder modulator (MZM). The electrical DPSK data consists of 500,000 raised-cosine shaped bits with 40 samples per bit. The generated DPSK signal is amplified and launched into a piece of fiber. Optical noises from optical amplifier are modeled as independent additive white Gaussian noises (AWGN) with zero mean and a power spectral density of $N_0/2$ for each polarization's in-phase and quadrature components. Fiber transmission link is modeled as a single-input, two-output setup [3]. The initial DPSK signal is split into two orthogonal polarization modes with γ being the relative power in the fast principle state of polarization. The sources for signal degradation, PMD and CD, are included. At the receiver, the signal is optically filtered by a Gaussianshaped 50-GHz optical-bandpass filter (OBPF). Then the optical signal is split into two branches by a 50/50 coupler. The two signal branches are demodulated by DIs with one-bit delay and two-bit delay respectively before they are detected by balanced detectors. After O-E conversion, the electrical signals are filtered by 7-GHz 4th-order Bessel electrical filters (EFs), sampled with one or two samples per bit, and decoded by using the conventional soft detection or MLSE as shown in Fig. 1. In the conventional detection, three differentially detected signal $q_T(k)$, $q_T(k)$ -1), and $q_{2T}(k)$, are used as the inputs to a 3×4 weighting matrix. The outputs of the matrix, q_{ii} , $i, j \in \{0, 1\}$, are

$$\begin{aligned} q_{00} &= q_T(k) + q_T(k-1) + q_{2T}(k), \quad q_{01} &= -q_T(k) + q_T(k-1) - q_{2T}(k), \\ q_{10} &= q_T(k) - q_T(k-1) - q_{2T}(k), \quad q_{11} &= -q_T(k) - q_T(k-1) + q_{2T}(k) \end{aligned}$$
(1)

For detection using MLSE, the sampled signal is firstly analog-to-digital (A/D) converted with the resolution of 5 bits. MLSE is a 4-state machine and Viterbi algorithm is employed. The metric PM(k) of MLSE is

$$PM(k) = PM(k-1) - \log(p(q_T(t) | b_{n-m}, ..., b_n)) \Big|_{t=T} - \log(p(q_{2T}(t) | b_{n-m}, ..., b_n)) \Big|_{t=T}$$

$$\left[-\log(p(q_{T}(t) | b_{n-m}, ..., b_{n}))|_{t=kT+T/2} - \log(p(q_{2T}(t) | b_{n-m}, ..., b_{n}))|_{t=kT+T/2}\right]$$
(2)

 (\mathbf{n})

with the initial metric in the channel training table obtained using nonparametric histogram method by a 200,000-bit training sequence. $p(q_T(t)|b_{n-m},...,b_n)$ and $p(q_{2T}(t)|b_{n-m},...,b_n)$ are the probability of $q_T(t)$ and $q_{2T}(t)$ giving the logical data $b_{n-m},...,b_n$, respectively. m is the memory length. Equation (2) assumes that the signal is sampled with two samples per bit. When one sample per bit is used, the terms in square brackets are omitted. The performance of the system is evaluated in terms of optical-signal-to-noise ratio (OSNR) penalty at bit error rate (BER) of 10^{-4} , which can be corrected below 10⁻¹⁵ using forward error correction.





3-chip DPSK (dashed), and 3-chip DPSK with MLSE of two samples per bit (solid).



3000

4000

Fig. 2 shows E_b/N_0 versus CD for 2-chip DPSK (dotted), pure 3-chip DPSK (dashed), and 3-chip DPSK with MLSE of two samples per bit (solid). $E_{\rm b}$ is the average power in one bit slot. From the figure, it is shown that the benefit by using pure 3-chip DPSK is not prominent for both back-to-back sensitivity and CD tolerance. By using MLSEequalized 3-chip DPSK, however, the CD tolerance of the DPSK signal is effectively improved. Negative penalty is achieved for cumulative CD less than 1500 ps/nm. At E_b/N_0 of 15 dB, the CD tolerance is enhanced from 1500 ps/nm to 2800 ps/nm. To further show the advantages of the proposed method, both the performance of MLSEequalized 3-chip DPSK and that of MLSE-equalized 2-chip DPSK are shown in Fig. 3. Dashed and solid lines





Figure 4: Required E_b/N_0 versus DGD for 2-chip DPSK (dotted), pure 3-chip DPSK (dashed), and 3-chip DPSK with MLSE of two samples per bit (solid). γ in the figure is 1/2.

Figure 5: Required E_b/N_0 versus DGD for 2-chip DPSK with MLSE and 3-chip DPSK with MLSE under one sample per bit (dashed) and two samples per bit (solid). γ in the figure is 1/2.

represent one sample per bit and two samples per bit, respectively. From Fig. 2&3, it is shown that the performance of MLSE depends on the chip number as well as the number of samples per bit. With one sample per bit, the performance improvement by using MLSE is not significant for both 2-chip DPSK and 3-chip DPSK. For 2-chip DPSK, the performance improvement by two-sample per bit MLSE is still limited compared to 2-chip DPSK without MLSE [5]. At E_b/N_0 of 15 dB, the CD tolerance is only enhanced from 1500 ps/nm to 1900 ps/nm. However, MLSE-equalized 3-chip DPSK significantly outperforms MLSE-equalized 2-chip DPSK and enhances the CD tolerance of the DPSK signal to 2800 ps/nm at E_b/N_0 of 15 dB, 1.5 times of that of MLSE-equalized 2-chip DPSK. Next, the performance of MLSE for 1st-order PMD compensation is investigated. Fig. 4 shows E_b/N_0 versus DGD for 2-chip DPSK (dotted), pure 3-chip DPSK (dashed), and 3-chip DPSK with MLSE of two samples per bit (solid). γ in the figure is 1/2. Similar to Fig. 2, compared to 2-chip DPSK, pure 3-chip DPSK cannot effectively improve the tolerance to PMD despite back-to-back sensitivity improvement. In contrast, MLSE of 3-chip DPSK can effectively improve the performance. For DGD of 100 ps, the penalty is upper-bounded by 1.6 dB. Fig. 5 shows the required $E_{\rm b}/N_0$ versus DGD for 2-chip DPSK with MLSE and 3-chip DPSK with MLSE under one sample per bit (dashed) and two samples per bit (solid). From the figure, it is shown that the performance of MLSE for PMD compensation is better than that for CD compensation irrespective of the sample number and the chip number. It is because 1st-order PMD results in linear distortions in the electrical domain. MLSE of 3-chip DPSK outperforms MLSE of 2-chip DPSK. At DGD of 100 ps, the penalties of one and two-samples per bit MLSE for 2-chip DPSK are around 8.5 dB and 4.2 dB, respectively. In contrast, these penalties are reduced to 5.5 dB and 1.6 dB for MLSEequalized 3-chip DPSK. Therefore, the proposed method is an effective method to further enhance the tolerance of the DPSK signal to CD and PMD. As a result, the transmission reach of the DPSK signal is significantly extended.

4. Conclusions

We have proposed to employ MLSE for 3-chip DPSK detection. It is shown that such method significantly outperforms pure 3-chip DPSK and MLSE of conventional 2-chip DPSK in CD and PMD compensation. At E_b/N_0 of 15 dB, the CD tolerance of 10-Gbit/s DPSK by using the proposed scheme is enhanced to 2800 ps/nm, around 1.5 times of that of MLSE-equalized 2-chip 10-Gbit/s DPSK. For 1st-order DGD of 100 ps, the E_b/N_0 penalty is upper-bounded by 1.6 dB, 2.6 dB penalty reduction compared to MLSE-equalized 10-Gbit/s 2-chip DPSK. Therefore, it is a promising technique to extend the transmission reach of the DPSK format in long-haul applications. This work was partially supported by a research grant from the Hong Kong Research Grants Council of Hong Kong, SAR, Project No. CUHK4110/06.

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