

Three-chip differential phase-shift keying maximum likelihood sequence estimation for chromatic-dispersion and polarization-mode-dispersion compensation

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We propose a novel three-chip differential phase-shift keying (DPSK) maximum likelihood sequence estimation (MLSE) for chromatic-dispersion (CD) and first-order polarization-mode-dispersion (PMD) compensation to extend the transmission reach of the DPSK signal. Such a technique searches the most probable path through the trellis for DPSK data sequence estimation by exploiting the phase difference between not only the adjacent optical bits but also the bits that are one bit slot apart. The proposed scheme significantly outperforms conventional two-chip DPSK MLSE in CD and PMD compensation. We show that the proposed three-chip DPSK MLSE can enhance the CD tolerance of 10 Gbit/s DPSK signal to 2.5 times of that by using two-chip DPSK MLSE and can bound the penalty for 100 ps differential group delay by 1.4 dB. © 2007 Optical Society of America

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An electronic equalizer such as maximum likelihood sequence estimation (MLSE) has recently attracted considerable interest for chromatic-dispersion (CD) and polarization-mode-dispersion (PMD) compensation because of its significant cost saving compared with all-optical compensation components and its adaptive compensation capability [1–3]. However, despite its effectiveness in extending the transmission reach of on-off keying modulation format, the conventional electronic equalizer provides limited CD tolerance improvement for the differential phase-shift keying (DPSK) format [1–3].

Recently, a new family of DPSK, multichip DPSK (MC-DPSK), was ported from wireless communication to optical communication [4–6]. By exploiting the phase difference between not only the adjacent optical bits but also the bits that are one or several bit slots apart, MC-DPSK soft detection improves the quantum limit sensitivity of incoherently detected DPSK approaching that of coherently detected phase-shift keying [4–6]. The least complex MC-DPSK scheme is three-chip DPSK soft detection. However, soft detection is based on a block-by-block decision and does not consider interblock interference. Therefore, this scheme provides only a slight improvement in CD and PMD tolerance compared with a two-chip DPSK hard decision.

In this paper, we propose a novel three-chip DPSK MLSE. We show that the proposed scheme can significantly enhance the CD and PMD tolerance of the DPSK signal.

Figure 1 shows the simulation model and the structures of three-chip DPSK soft detection and the proposed three-chip DPSK MLSE. A continuous-wave light is phase modulated by a 10 Gbit/s DPSK data train using a Mach-Zehnder modulator. The DPSK data train consists of 500,000 raised-cosine shaped bits with 40 samples/bit. The generated DPSK signal

is launched into a piece of fiber. In the fiber link, the DPSK signal is split into two orthogonal polarization modes, with $\gamma=0.5$ being the relative power in the fast principal state of polarization. The sources for signal degradation, CD and PMD, are included. At the receiver, the signal is optically preamplified and filtered by a 50 GHz Gaussian-shaped optical band-pass filter. Optical noise from the optical preamplifier is modeled as complex additive white Gaussian noise with zero mean and a power spectral density of N_0 for each polarization component. The signal is then split into two branches by a 50/50 coupler. The signals of the two branches are demodulated by delay interferometers with one- and two-bit delays and detected by

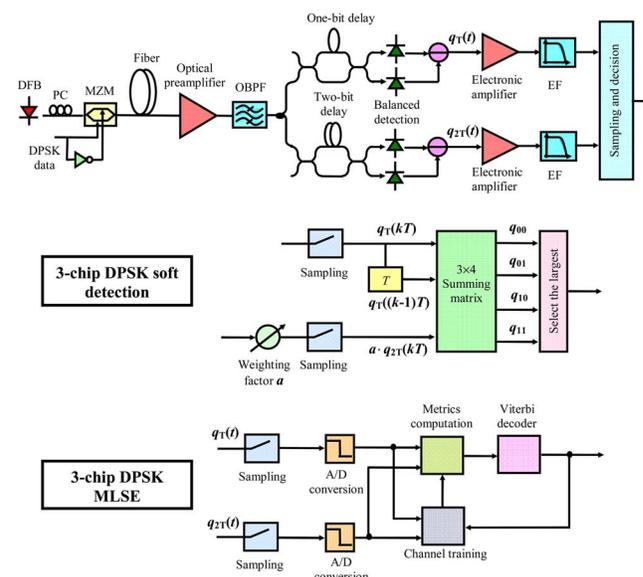


Fig. 1. (Color online) Simulation model and the structures of three-chip DPSK soft detection and the proposed three-chip DPSK MLSE.

balanced detectors. After O–E conversion, the detected signals, $q_T(t)$ and $q_{2T}(t)$, are electronically amplified, filtered by 7 GHz fourth-order Bessel electronic filters, and sampled.

For three-chip DPSK soft detection, maximum likelihood principle is employed for block-by-block decision [4]. An example with a transmitted pattern (π 0 π π 0 π 0) is used to illustrate three-chip DPSK soft detection in Fig. 2. Three signals, $q_T(kT)$, $q_T((k-1)T)$, and $a \cdot q_{2T}(kT)$, are used as the inputs to a 3×4 summing matrix, where a is the weighting factor to evaluate the importance of $q_{2T}(kT)$ in data decision [6]. The matrix outputs, q_{ij} , i and $j \in \{0, 1\}$, are

$$\begin{aligned} q_{00} &= q_T(kT) + q_T((k-1)T) + a \cdot q_{2T}(kT), \\ q_{01} &= -q_T(kT) + q_T((k-1)T) - a \cdot q_{2T}(kT), \\ q_{10} &= q_T(kT) - q_T((k-1)T) - a \cdot q_{2T}(kT), \\ q_{11} &= -q_T(kT) - q_T((k-1)T) + a \cdot q_{2T}(kT). \end{aligned} \quad (1)$$

The maximum-likelihood decision is to find the largest q_{ij} , and its corresponding indices are the best estimation of the 2-bit DPSK data (b_{k-1} , b_k).

On the other hand, sequence estimation is employed in the proposed scheme. $q_T(t)$ and $q_{2T}(t)$ are sampled with two samples per bit and analog-to-digital converted with a resolution of 5 bits. The samples from both $q_T(t)$ and $q_{2T}(t)$ are simultaneously exploited in the initial channel training and the metrics computation. The metric of three-chip DPSK MLSE, $PM(k)$, is

$$\begin{aligned} PM(k) &= PM(k-1) - \sum_{t_j} \log(p(q_T(t_j)|b_{k-m}, \dots, b_k)) \\ &\quad - a \cdot \sum_{t_j} \log(p(q_{2T}(t_j)|b_{k-m}, \dots, b_k)). \end{aligned} \quad (2)$$

For $q_T(t_j)$, $t_j = (k-m/2)T$, $(k-(m+1)/2)T$, or $(k-(m-1)/2)T$. For $q_{2T}(t_j)$, $t_j = (k-m/2)T$, $(k-(m-1)/2)T$, or $(k-(m-2)/2)T$. $p(q_i(t_j)|b_{k-m}, \dots, b_k)$, with i being T or $2T$, is the probability of the sampled $q_i(t)$ signal value at $t=t_j$ giving the DPSK logical data b_{k-m}, \dots, b_k . m is the memory length. The initial metrics in the channel training table are obtained using a nonparametric histogram method by a 200,000-bit training sequence. Notice that, unlike the joint MLSE structure, which estimates the data of different tributaries in multibit modulation format simultaneously [7], three-chip DPSK MLSE employs the redundant information from two input branches for one bit per symbol DPSK data estimation. Therefore, its compu-

tation complexity is proportional to 2^{m+1} rather than 4^{m+1} , that of a joint MLSE. The performance is evaluated in terms of required E_b/N_0 (required photon number per bit before preamplification) to achieve a bit error rate of 10^{-4} , where E_b is the optical average power in one bit slot after optical preamplification.

First, the effect of the weighting factor a on the performance of three-chip DPSK soft detection and three-chip DPSK MLSE is investigated. Figure 3(a) shows the required E_b/N_0 (in dB) versus CD by using three-chip DPSK soft detection (circles) and three-chip DPSK MLSE with $m=4$ (triangles) under $a=1$ (solid curves) and optimal a value for each CD value (dashed curves). From the figure, it is shown that, by using three-chip DPSK MLSE, the CD tolerance of the DPSK signal is significantly enhanced compared with that obtained by using three-chip DPSK soft detection. The CD tolerance of the DPSK signal under $a=1$ (solid curve) is very close to that under optimal a value (dashed curves), irrespective of three-chip DPSK detection method. Figure 3(b) depicts the required E_b/N_0 (in dB) versus a by using three-chip DPSK soft detection (circles) and three-chip DPSK MLSE with $m=4$ (triangles) when the CD values are 1250 ps/nm (solid curves) and 2500 ps/nm (dashed curves). From the figure, it is shown that the optimal a values change with CD values [6]. Similar conclusions from Figs. 3(a) and 3(b) can also be obtained for the PMD tolerance of the DPSK signal. Figure 4(a) shows the required E_b/N_0 (in dB) versus differential group delay (DGD) by using three-chip DPSK soft detection (circles) and three-chip DPSK MLSE with $m=4$ (triangles) under $a=1$ (solid curves) and optimal a value for each DGD value (dashed curves). Figure 4(b) depicts the required E_b/N_0 (in dB) versus a by using three-chip DPSK soft detection (circles) and three-chip DPSK MLSE with $m=4$ (triangles) when the DGD values are 40 ps (solid curves) and 80 ps (dashed curves). From Figs. 3 and 4, for both three-chip DPSK detection methods, it is concluded that $a=1$ can be used to eliminate the complexity of weighting factor optimization with negligible performance degradation.

To further show the advantages of the proposed scheme in CD and PMD compensation, Fig. 5(a) shows the required E_b/N_0 (in dB) versus CD for the two-chip DPSK signal (solid curves) and the three-chip DPSK signal under the weighting factor $a=1$ (dashed curves). The circles, triangles, and squares represent the detection methods without MLSE (two-chip DPSK optimal threshold detection/three-chip DPSK soft detection), with MLSE under memory

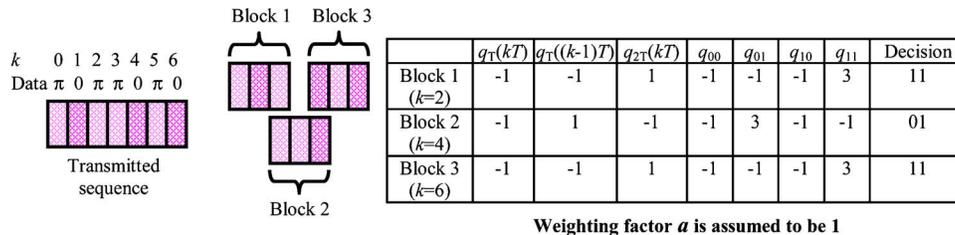


Fig. 2. (Color online) Example of three-chip DPSK soft detection.

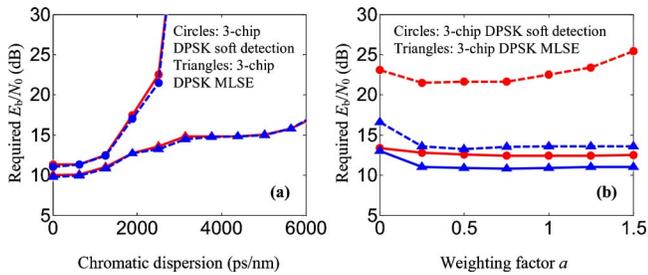


Fig. 3. (Color online) (a) Required E_b/N_0 (dB) versus CD obtained by using three-chip DPSK soft detection (circles) and three-chip DPSK MLSE with $m=4$ (triangles) under $a=1$ (solid curves) and optimal a value for each CD value (dashed curves). (b) Required E_b/N_0 (in dB) versus a obtained by using three-chip DPSK soft detection (circles) and three-chip DPSK MLSE with $m=4$ (triangles) when the CD values are 1250 ps/nm (solid curves) and 2500 ps/nm (dashed curves).

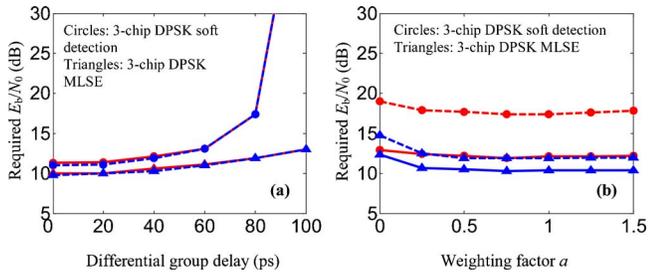


Fig. 4. (Color online) (a) Required E_b/N_0 (in dB) versus DGD obtained by using three-chip DPSK soft detection (circles) and three-chip DPSK MLSE with $m=4$ (triangles) under $a=1$ (solid curves) and optimal a value for each DGD value (dashed curves). (b) Required E_b/N_0 (in dB) versus a obtained by using three-chip DPSK soft detection (circles) and three-chip DPSK MLSE with $m=4$ (triangles) when the DGD values are 40 ps (solid curves) and 80 ps (dashed curves).

length $m=2$, and with MLSE under $m=4$, respectively. From the figure, it is shown that, compared with two-chip DPSK optimal threshold detection (circles and solid curves), three-chip DPSK soft detection (circles and dashed curves) exhibits only slight CD tolerance improvement because it does not consider interblock interference. By employing sequence estimation, two-chip DPSK MLSE achieves higher CD tolerance than three-chip DPSK soft detection. However, its performance in CD compensation for the DPSK signal is still limited [3], with CD tolerance about 1900 ps/nm at E_b/N_0 of 15 dB, irrespective of two-chip DPSK MLSE's memory length. In contrast, three-chip DPSK MLSE significantly outperforms conventional two-chip DPSK MLSE in CD compensation. At E_b/N_0 of 15 dB, the CD tolerance by using three-chip DPSK MLSE is enhanced to 2800 and 5000 ps/nm for memory length $m=2$ and 4, respectively. These values are about 1.5 times and 2.5 times of those by using conventional two-chip DPSK MLSE. Next, the performance of the proposed three-chip DPSK MLSE for first-order PMD compensation is investigated. Figure 5(b) shows the required E_b/N_0 (in dB) versus DGD for two-chip DPSK signal (solid curves) and three-chip DPSK signal under $a=1$

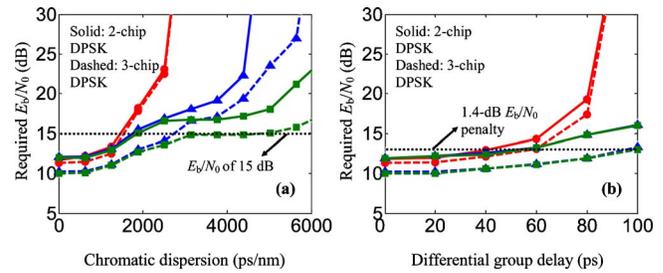


Fig. 5. (Color online) Required E_b/N_0 (in dB) versus (a) CD and (b) DGD for two-chip DPSK signal (solid curves) and three-chip DPSK signal under the weighting factor $a=1$ (dashed curves). The circles, triangles, and squares represent the detection methods without MLSE (two-chip DPSK optimal threshold detection/three-chip DPSK soft detection), with MLSE under memory length $m=2$, and with MLSE under $m=4$, respectively.

(dashed curves). The circles, triangles, and squares represent the detection methods without MLSE, with MLSE under $m=2$, and with MLSE under $m=4$, respectively. From the figure, it is shown that, similar to Fig. 5(a), three-chip DPSK MLSE significantly outperforms the other detection methods in PMD compensation. For DGD of 100 ps, the E_b/N_0 penalties obtained by using three-chip DPSK MLSE with $m=2$ and 4 are bounded by 1.6 and 1.4 dB respectively, which correspond to 2.6 and 2.8 dB penalty reduction compared with those obtained by using two-chip DPSK MLSE, where the E_b/N_0 penalty is with respect to the back-to-back E_b/N_0 ($E_b/N_0=11.8$ dB) of the two-chip DPSK optimal threshold detection.

We have proposed a novel three-chip DPSK MLSE to extend the transmission reach of the DPSK signal in high-speed optical transmission applications. The proposed technique significantly outperforms conventional two-chip DPSK MLSE in CD and first-order PMD compensation. We show that at E_b/N_0 of 15 dB, the proposed method can enhance the CD tolerance of 10 Gbit/s DPSK signal to 5000 ps/nm, 2.5 times of that by using two-chip DPSK MLSE. For PMD compensation, the proposed method can bound the E_b/N_0 penalty for 100 ps DGD by 1.4 dB, a 2.8 dB penalty reduction compared with that obtained by using two-chip DPSK MLSE.

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