Optimization of Microring-based Optical Interconnection Configurations for the Reduction of Power Consumption and Insertion Loss

Piu-Hung Yuen and Lian-Kuan Chen
Department of Information Engineering, The Chinese University of Hong Kong, Shatin, N.T., Hong Kong SAR, China
Tel: +852-2609-8385, Fax: +852-2603-5032, Email: yph010@ie.cuhk.edu.hk

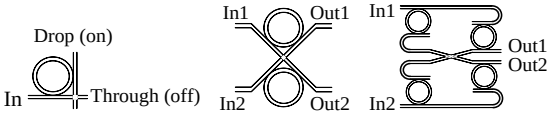
Abstract: With the objectives of reducing power consumption and average insertion loss, optimal configurations for optical interconnection are determined, leveraging the asymmetric behaviors at cross/bar states of microring switching element. Besides, a novel heuristic is proposed.
OCIS codes: (200.0200) Optics in Computing; (200.4650) Optical Interconnects

1. Introduction

There has been an increased research interest on networks-on-chip architectures for growing computation-intensive applications and high-performance multi-core computing systems recently. With the growing trend of number of cores per chip and computation resources per chip, the advancement or alternative for conventional metallic interconnections is essential to meet the demands of high-bandwidth capacity, low power consumption, compact footprint and high scalability. A report from ITRS pointed out that optical interconnections based on CMOS-compatible silicon photonic is an alternative to conform to the above requirements [1]. The carrier-injection-based silicon microring resonators is a promising candidate to build large scale integrated optical interconnections using 2×2 switching elements (SEs) due to its very compact footprint and sub-nanosecond switching time [2]. However, current technology for a 2×2 SE of microring requires non-negligible power consumption at cross/bar states on average [3]. Intrinsic insertion loss also limits the number of successive switching elements per switching path [4,5]. In other words, asymmetric loss characteristics of SEs limit the scalability of optical interconnections. Hence, the aim of this paper focuses on the reduction in overall power consumption and average total insertion loss per path.

2. Asymmetric behaviors at cross/bar states

Power consumption: A microring with a simple architecture as shown in Fig. 1(a) (labeled 1B-SE) can be designed to be either on/off-resonance by default when there is no electrical power supplied [6]. Therefore, a 2x2 switch which uses two rings as shown in Fig. 1(b) may have unequal power consumption at cross/bar states. One recent experimental result for the average power consumption of a 1B-SE is 100μW [7]. Another experimental measurement shows that the SE architecture in Fig. 1(b) (labeled 2B-SE) requires nearly no power at cross state and less than 500μW at bar state [8]. In this study, we assume that the power consumption of a 2B-SE is 0μW at cross (bar) state and 200μW at bar (cross) state without loss of generality.



(a) 1B-SE (b) 2B-SE (c) 2D-SE
Fig.1. Microring-based switching elements

Insertion loss: Due to the propagation loss inside the ring waveguide and the coupling between the busline and the ring, 1B-SE exhibits asymmetric insertion loss at on/off resonance [4,5]. In [5], it is shown that input signal suffers significant power loss of 1.4dB and nearly negligible power loss of 0.1dB when the ring is in drop and through configurations respectively. In that particular case, the insertion loss for a 2B-SE at bar state is 1.4dB and that at cross states is 0.2dB. To resolve the issue of asymmetries, a new architecture of SE is proposed as Fig. 1(c) (labeled 2D-SE) in [5]. It achieves equal insertion loss of 1.5dB at both bar state and cross state. Albeit the asymmetric insertion loss is resolved, the total insertion loss of a large scale optical interconnection has not been optimized and a 2D-SE requires double complexity than a 2B-SE in terms of number of microrings used. In this study, 2B-SE will be used as a building block for large scale optical interconnections.

3. Principle

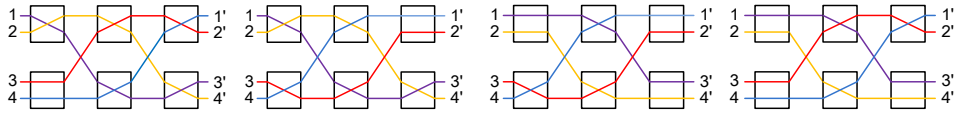
The following describes a generic principle in determining the optimal switch configurations of total power consumption and average total insertion loss per path of classical switch architectures. A large scale of microring-based optical interconnection which is constructed by cascading N of 2B-SEs will be examined. In an $n\times n$ switch, there are 2^N sets of configurations to satisfy $n!$ traffic matrices, T. For each traffic matrix, there may be more than one possible configuration as $2^N > n!$. A 4×4 Benes switch is selected as an example for illustration since it exhibits minimum complexity among various nonblocking architectures. For a given traffic matrix, all possible configurations can be found by the equation of $T=S_1\times E_1\times S_2\times E_2\times S_3$. S_1, S_2 and S_3 are stage matrices, consisting of the switch configurations of the 2B-SEs at the first, second and third stage, respectively, where E_1 and E_2 are edge

matrices for the interconnection between each stage. Hence, T can be expressed as Eq. (1). s_{ij} and s_{ij}' represent the bar/cross state of the j^{th} 2B-SE at stage-i, where s_{ij}=1 (0) denotes the switch is at bar (cross) state. It should be noted that s_{ij} and s_{ij}' are binary and complements of each other. First, the following traffic matrix, T is analyzed.

$$T = \begin{pmatrix} s_{11} & s_{11}' & 0 & 0 \\ s_{11}' & s_{11} & 0 & 0 \\ 0 & 0 & s_{12} & s_{12}' \\ 0 & 0 & s_{12}' & s_{12} \end{pmatrix} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} s_{21} & s_{21}' & 0 & 0 \\ s_{21}' & s_{21} & 0 & 0 \\ 0 & 0 & s_{22} & s_{22}' \\ 0 & 0 & s_{22}' & s_{22} \end{pmatrix} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} s_{31} & s_{31}' & 0 & 0 \\ s_{31}' & s_{31} & 0 & 0 \\ 0 & 0 & s_{32} & s_{32}' \\ 0 & 0 & s_{32}' & s_{32} \end{pmatrix} \quad (1)$$

$$T = \begin{pmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix}$$

(a)



(b) (c) (d) (e)

Fig. 2. (a) an example of T and (b)-(e) the possible switch configurations

The operating power for a 2B-SE at bar state, P_b, is assumed to be higher than that at cross state, P_c, without loss of generality. Different configurations, depending on the number of cross/bar states, result in different total power consumption. There are four possible configurations after solving the equation for the T in Fig. 2(a). The two configurations in Fig. 2(b) and (c) are the optimal switch configurations of total power consumption = P_b+5P_c, whereas the other two in (d) and (e) are of high total power consumption, 3P_b+3P_c. When the number of ports increases, the above equations are still valid by multiplying more stage matrices and edge matrices. Hence, the total power consumption of an n×n Benes switch can be optimized by configuring the 2B-SEs appropriately. In simulations, we generated 2^N sets of configurations up to 100,000 sets for large value of N to match certain traffic matrix, in which the switch configuration with minimum total number of bar state switches will be selected as the optimal configuration. The average number of bar state switches for an n×n switch is the average of number of bar state at optimal configuration for each traffic matrix.

Regarding the optimal configuration for the reduction of average total insertion loss per path in 2B-SE, we apply the principle in a similar manner with the insertion loss at bar state, IL_b, higher than that at cross state, IL_c. The objective functions for minimizing the total power consumption, P_{T_min}, and the average total insertion loss per path, IL_{T_min}, are to minimize the total number of bar state switches. Therefore, the corresponding objective functions are $P_{T\_min} = \min_{s_{ij}, s_{ij}' \in \{0,1\}} \left\{ P_b \sum_{i,j} s_{i,j} + P_c \sum_{i,j} s_{i,j}' \right\}$ and $IL_{T\_min} = \min_{s_{ij}, s_{ij}' \in \{0,1\}} \left\{ [IL_b \sum_{i,j} s_{i,j} + IL_c \sum_{i,j} s_{i,j}'] / n \right\}$, respectively for classical switch architecture. The two objectives can be achieved simultaneously by minimizing the total number of bar state switches which is $\sum_{i,j} s_{i,j}$.

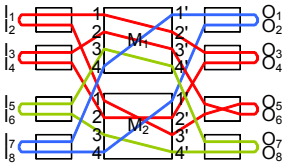
4. Heuristic

To find the optimal configuration with shorter computation time, we develop a novel heuristic to minimize the number of bar state switches. It presents the iterative procedure for changing cross state to bar state recursively for Benes architecture for each loop.

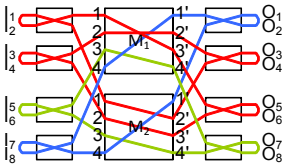
Step 1: For a given initial configuration, the inputs and outputs are connected by looping algorithm as shown in Fig. 3(a). 2×2 SEs at the first and third stage in different loops are independent in changing states.

Step 2: For each loop, all SEs at the first stage (e.g. SE of port I_1, I_2; SE of port I_3, I_4) and the third stage (e.g. SE of port O_3, O_4; SE of port O_5, O_6) are changed to their opposite states at the same time if there are more bar state SEs in that loop. Otherwise, the change of configuration for SEs at the first and third stage is finished.

Step 3: As shown in Fig. 3(a), if the loop passes two central modules (M_1 & M_2), input-output pairs in the same loop at M_1 (ports in M_1: 1→2'; 2→3') will interchange input-output pairs in the same loop at M_2 (ports in M_2: 1→3'; 2→2'). Fig. 3(b) shows the switch configuration after changing bar state to cross state.



(a)



(b)

Fig. 3. Looping algorithm in Benes architecture

Step 4: An n×n Benes switch can be decomposed into two N/2×N/2 modules in the middle consisting of 2×2 SEs at the first and third stage. An N/2×N/2 module can then be broken down into three stages consisting of 2×2 SEs at the first and third stage and repeat from ***step 1***. The change is performed recursively from the outer stages to the inner stages until the central module become 2×2 SEs. After the heuristic, the number of bar state switches is minimized.

5. Results and Analysis

Using the measurement values as mentioned in section 2, the power saving using the optimal switch configuration for a given switch size is obtained and compared with the average power consumption without optimization. The results in Fig. 4(a) show that significant power savings for Benes, Spanke-Benes and Crossbar switch can be achieved for a 128×128 switch. The curve shows that the power saving of the optimal configuration increases with

the number of ports. Crossbar switch has the best performance due to its high flexibility. Fig. 4(b) depicts the absolute power consumption for different switch architectures. It increases linearly with the number of ports. Albeit Crossbar switch achieves a high power saving, its absolute power consumption is almost double of Benes switch for 128×128 switch size due to the high complexity of Crossbar switch.

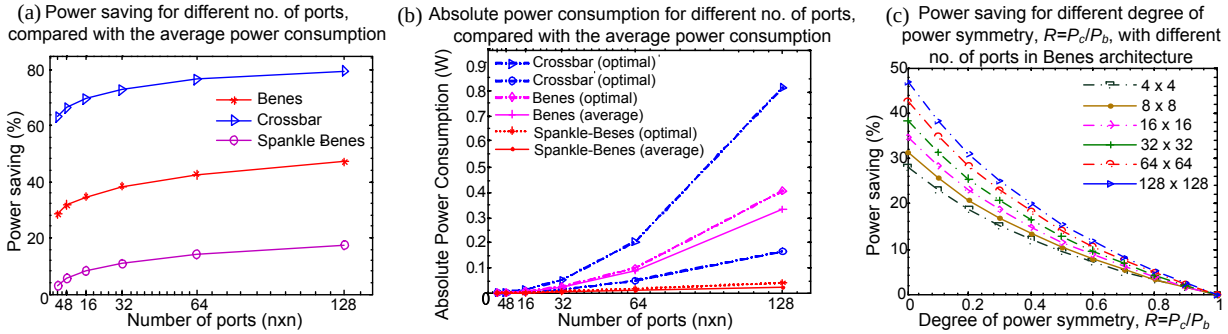


Fig. 4. (a)-(c) Simulation results for the reduction of power consumption in optimal configurations with different number of ports

We further investigate the effect of symmetry in cross/bar state on the relative power saving. R is defined as $R=P_c/P_b$. We denote C to be the sum of P_c and P_b, $C=P_c+P_b$. P_c and P_b can be written as $P_c=CR/(1+R)$ and $P_b=C/(1+R)$, respectively. Without optimization, since each traffic demand is equally probable, the number of bar sate switches and cross switches both equals to $N/2$ on average. Hence, the total power consumption before and after optimization are $P_{T\_org}=C(N/2+N/2)/2=CN/2$ and $P_{T\_opt}=P_c(N-N_{b\_opt})+P_bN_{b\_opt}$ respectively, where N_{b_opt} is the minimum total number of bar state switches at optimal configuration. The relative power saving, r is then simplified as $r=\frac{P_{T\_org}-P_{T\_min}}{P_{T\_org}}=1-\left[\frac{R}{1+R}\right]\left[2-\frac{2N_b}{N}\right]-\left[\frac{1}{1+R}\right]\left[\frac{2N_b}{N}\right]$. It is observed that the relative power saving depends on the degree of power symmetry, R, and the ratio of switch in bar state, N_b/N. Thus, optical interconnections with the same R in SE, achieve the same relative power saving regardless of the absolute power consumption for each SE.

Fig. 4(c) shows the results of power saving for different degree of power symmetry. Results reveal that the higher the degree of power symmetry, the lower the power saving. Power saving attains its maximum when $P_c=0$. In other words, it is favorable to fabricate a microring SE with higher asymmetry in power consumption at cross/bar states for lower overall power consumption. Total insertion loss per path is a dominant factor for the scalability of optical interconnections. The results in Fig. 5 show the average total insertion loss per path increases with the number of ports in Benes architecture. The average total insertion loss per path using 2B-SE achieves 3.65dB improvement while the optimal average total insertion loss using 2B-SE in worst-case path (WCP) has 7.2dB improvement for 128×128 switch size at optimal switch configurations compared with the baseline values without optimization. There is no optimization for microring-based interconnection using 2D-SE because it attains the same insertion loss at cross/bar states.

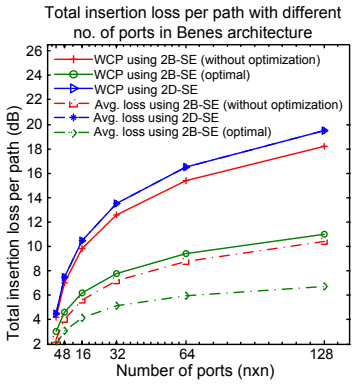


Fig. 5. Total insertion loss per path with different number of ports in Benes architecture

6. Conclusions

We successfully demonstrated that with optimized switch configuration overall power consumption and average total insertion loss per path can be reduced for microring-based interconnection. A new heuristic is also proposed to reduce the computation time for the optimal switch configuration. The results also depict that the optimal average total insertion loss per path using 2B-SE achieve 3.65dB improvement for 128×128 switch size. The optimal average total insertion loss using 2B-SE in worst-cast path is shown to be 7.2dB less than the baseline values without optimization. This work is supported in part by RGC GRF CUHK410908.

7. References

[1] S. I. Association, "The International Technology Roadmap for Semiconductors," (2009).
[2] A. W. Poon et al., "Cascaded microresonator-based matrix switch for silicon on-chip optical interconnection," in Proc. IEEE **97**, 1216-1238 (2009).
[3] A. Shacham et al., "Photonic networks-on-chip for future generations of chip multiprocessors," IEEE Trans. Comput. **57**, 1246 (2008).
[4] B. G. Lee et al., "All optical comb switch for multiwavelength message routing in silicon photonic networks," IEEE Photon. Technol. Lett.,**20**, 767–769 (2008).
[5] A. Bianco et al., "Scalability of Optical Interconnects Based on Microring Resonators," IEEE Photon. Technol. Lett. **22**, 1081-1083 (2010).
[6] N. Kirman et al., "A power-efficient all-optical on-chip interconnect using wavelength-based oblivious routing," ASPLOS, 15-28 (2010).
[7] B. A. Small et al., "Multiple-wavelength integrated photonic networks based on microring resonator devices", J. Opt. Netw. **6**, 112–120, (2007).
[8] A. Shacham et al., "On the Design of a Photonic Network-on-Chip," IEEE NOCS 2007, 53-64 (2007).