Optimization of Microring-based Interconnection Configurations for Reduction of Power Consumption, Insertion Loss and Crosstalk

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Abstract

There is an increasing research interest on networks-on-chip architectures for growing computation-intensive applications and high-performance multi-core computing systems recently. With the growing trend of number of cores per chip and computation resources per chip, the advancement for conventional interconnections is essential to meet the demands of high-bandwidth capacity, low power consumption, compact footprint and high scalability. A report from ITRS pointed out that optical interconnections based on Complementary Metal Oxide Semiconductor (CMOS)-compatible silicon photonics is an alternative to conform to the above requirements. The carrier-injection-based silicon microring resonators is a promising candidate to build large-scale-integrated optical interconnections using 2×2 switching elements due to its very compact footprint and potential sub-nanosecond switching time.

However, the scalability of microring-based interconnection is limited by issues including power consumption, insertion loss, nonuniformity and crosstalk. Current technology for a 2×2 switching elements of microring requires non-negligible power consumption at cross/bar states on average. Intrinsic insertion loss also limits the number of successive switching elements per switching path. In other words, asymmetric loss characteristics of switching elements limit the scalability of optical interconnections. Also, the nonuniformity of optical power is an important issue to be considered in meeting the requirement of a large-scale optical interconnection. Last, as in each 2×2 switching element, there is an optical power leakage to the non-intended output-port and thus it creates many possible crosstalk powers at each output-port. This total crosstalk at output is severe and needs to be reduced for the scalability consideration of microring-based interconnection. Hence, the aim of this thesis focuses on the reduction in overall power consumption, average total insertion loss per path, average nonuniformity of optical power and total crosstalk at each

output-port.

In this thesis we firstly review the background of microring resonator architecture and microring-based interconnections. The severe asymmetric behaviors limiting the scalability of interconnection are discussed. Then we review previous work dedicated to the scalability issues. By leveraging the asymmetric characteristics at cross/bar states of microring switching elements, we then propose an efficient model to find the optimum switching configuration for minimizing the total power consumption and the average insertion loss per path. Heuristics is also proposed to minimize the number of cross state switching elements with a shorter computation time. The results depict that the optimum average total insertion loss per path using 2B-SE achieve a 3.65-dB improvement for 128×128 switch size. The optimum average total insertion loss using 2B-SE in the worst-cast path is shown to be 7.2 dB less than the baseline values without optimization. Furthermore, simulation results show that regarding the nonuniformity in the worst case of the worst case, with the optimum switching configuration, the best improvement is 9.6 dB; the average improvement is 8.7 dB and the least improvement is 7.2 dB for 128×128 switch size. On the other hand, for the total crosstalk per path, simulation results show that the optimum switching configuration can achieve a 1.87-dB improvement for 128×128 switch size on average, compared with the average case without optimization. Also, the total crosstalk has a 2.43-dB improvement for 128×128 switch size in the worst case.

摘要

最近社會對計算密集型應用程序和高性能的多核計算系統的研究興趣增加。隨著每片芯片和計算資源的核心數量不斷增長的趨勢，更好的金屬互連或其他替代是至關重要的。這亦要滿足高帶寬，低功耗，細小體積和高擴展性的要求。ITRS 的報告指出，兼容 CMOS 的矽光子光互連是一種替代，它符合上述要求，包括體積細少和只需納秒的開關時間，所以矽微環諧振器是具潛能被用爲 2×2 開關元件來建立大規模集成光互連。

然而，微環互連的可擴展性可能受限制的，其中四個關注點包括總功耗，插入損耗，光功率不均勻和總串擾。2×2 切換微環需要一定的功耗，而插入損耗也限制了每條切換路徑所經過的開關元件的數量。換句話說，開關元件在交互/直行狀態下的非相等損失限制了光互連的可擴展性。此外，在考慮滿足大型光互連的要求，光功率的不均勻性是一個重要的問題。最後，在每個 2×2 開關元件，輸出光功率洩漏對大型的光互連的輸出造成許多可能的串擾。這在輸出端口的總串擾是十分嚴重，它會減少微環互連的可擴展性。因此，本論文的目的著重於降低整體功耗，路徑的總插入損耗，每個輸出端口的光功率不均勻和每個輸出端口的總串擾。

在這篇論文中，我們首先回顧微環諧振器的結構和微環互連的背景。限制互連的可擴展性也將被討論。然後，我們將回顧以前的研究，致力於解決可擴展性問題。通過利用微環開關元件的不相等特徵，我們提出一個有效的模型以找到最佳的開關配置，來減少總功耗和每通道的平均插入損耗。此外，我們還提出

一個快速的算法，以較短的計算時間減少交叉狀態開關元件數量。

另外，我們亦研究盡量減少不同的輸出端口的光功率不均勻問題及每個輸出端口的總串擾，以及最差路徑的光功率不均勻和最差輸出端口的的總串擾。仿真結果表明，我們的方案可以在整體功耗，平均路徑的總插入損耗，光功率的不均勻性，及每個輸出端口的總串擾，都有顯著的減少。結果顯示，在 128×128 的光互連下，每個路徑的最優平均總插入損耗可達 3.65 分貝的改善：而在最差的總插入損耗的路徑下，最優平均總插入損耗可達 7.2 分貝的改善。另外，結果亦指出在最差的光功率的不均勻情況下，最佳的改善爲 9.6 分貝，平均提高 8.7 分貝，最少亦可有 7.2 分貝的改善。而在每個路徑的總串擾，仿真結果表明輸出端口的總串擾可以有 1.87 分貝的改善，而在最差的總串擾情況下亦有 2.43 分貝的改善。

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Chapter 1

Introduction

1.1 Background

There is an increasing research interest on networks-on-chip architectures for growing computation-intensive applications and high-performance multi-core computing systems recently. With the growing trend of number of cores per chip and computation resources per chip, the advancement for conventional interconnections is essential to meet the demands of high-bandwidth capacity, low power consumption, compact footprint and high scalability. Silicon-on-insulator (SOI) technology is attractive for realizing photonic integrated circuit interconnections thanks to its characteristics of high index contrast and complementary metal-oxide-semiconductor (CMOS) compatibility.

Recently, a report from ITRS pointed out that optical interconnections based on CMOS-compatible silicon photonic is an alternative to conform to the above requirements [1]. The carrier-injection-based silicon microring resonators is a promising candidate to build large-scale-integrated optical interconnections using 2×2 switching elements (SEs) due to its very compact footprint and potential sub-nanosecond switching time [2]. With the growing demand for short-range optical interconnection technology at the board-to-board or chip-to-chip levels, it can be envisioned that microring-based interconnection will play an important role in the photonics device trend for the next decade.

1.2 Overview of microring resonators and microring-based optical interconnection

Microring resonators can perform passive operations like multiplexing and filtering. It can also work actively, such as electro-optic, all-optical, and thermo-optic switching and modulation. For a better understanding of microring-based optical interconnection, we now give a brief introduction for microring resonators. Some key features and physical design will be discussed.

There are several basic characteristics of microring resonators. The main feature of a microring resonator is that its transfer function is identical to that of a Fabry-Perot cavity. It has been demonstrated that a single microring resonator can perform comb switching for Wavelength-Division Multiplexing (WDM) applications [3]. The free-spectral range (FSR) of a microring resonator is relatively small and is approximately equal to the spacing (0.8 nm) in Dense WDM (DWDM). Thus, a large number of wavelength channels can be simultaneously switched on and off in microring resonators. For example, one study showed that a single microring resonator can achieve all-optical switching simultaneously for 20 continuous-wave wavelength channels [4].

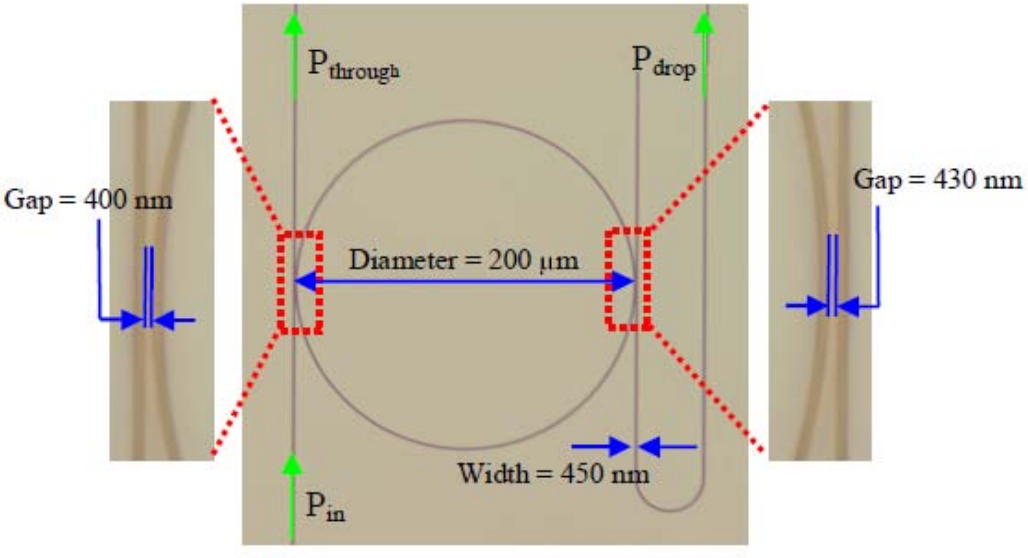
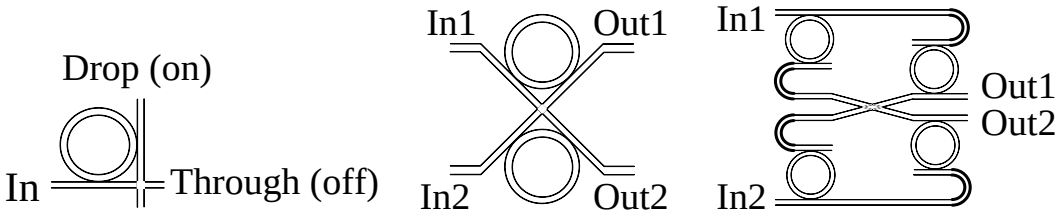


Fig. 1.1 Top-view microscopic picture of a microring resonator [3]

For a typical design of a microring resonator, a circularly-bent waveguide forms a ring with a diameter of typically ten to thousand times the wavelength. This diameter value depends on the refractive index contrast of the waveguide materials. As shown in Fig. 1.1, there are two straight waveguides near the microring resonator [3]. These two nearby waveguides are designed as the input and output path for the optical signal. Thus, four input/output-ports are available for the case of two waveguides near the microring.

As mentioned before, a microring resonator can be used to perform all-optical compact silicon comb switching as depicted in Figure 1.1. Microring tuning can be achieved by pumping optical pulses into the ring. In addition, by carrier injection or thermal tuning, it is also possible to shift the desired transfer function.

1.3 Asymmetric characteristics of microring switching elements



(a) 1B-SE (b) 2B-SE (c) 2D-SE

Fig. 1.2. Microring-based switching elements

A. Power consumption

A microring with a simple architecture as shown in Fig. 1.2(a) (labeled 1B-SE) can be designed to be either on/off-resonance by default when there is no electrical power supplied [7]. Therefore, a 2×2 switching element which uses two rings as shown in Fig. 1.2(b) may have unequal power consumption at cross/bar states.

One recent measurement value for the average power consumption of a 1B-SE is 100 μW [8]. Another measurement shows that the SE architecture in Fig. 1.2(b) (labeled 2B-SE) requires nearly no power at cross state and less than 500 μW at bar state [9].

In this study, we assume that the power consumption of a 2B-SE is 0 μW at cross (bar) state and 200 μW at bar (cross) state without loss of generality.

B. Insertion loss

Due to the propagation loss inside the ring waveguide and the coupling between the busline and the ring, 1B-SE exhibits asymmetric insertion loss at on/off resonance [4,6]. In [6], it is shown that input signal suffers significant power loss of 1.4 dB and nearly negligible power loss of 0.1 dB when the ring is in drop and through configurations, respectively. In that particular case, the insertion loss for a 2B-SE at bar state is 1.4 dB and that at cross state is 0.2 dB. To resolve the issue of asymmetries, a new architecture of SE is proposed as Fig. 1.2(c) (labeled 2D-SE) in [6]. It achieves equal insertion loss of 1.5 dB at both bar state and cross state. Albeit the asymmetric insertion loss is resolved, the total insertion loss of a large scale optical interconnection has not been optimized and a 2D-SE exhibits double complexity than a 2B-SE in terms of number of microrings used.

In this study, 2B-SE will be used as a building block for large scale optical interconnections.

C. Nonuniformity

For 2B-SE architecture, there is no nonuniformity issue at cross/bar states. However, in a microring-based optical interconnection based on 2B-SE, the optical power at each output-port is different since each lightpath suffers different insertion loss. In other words, due to the asymmetric insertion loss at cross/bar states, nonuniformity of optical power occurs when cascading the switching elements to build an optical interconnection. The architecture of 2D-SE shown in Fig. 1.2(c) solves the

nonuniformity issue at the expense of double complexity in terms of the number of microring used and the scheme will be reviewed in detail in Chapter 2.

D. Crosstalk

For each 2B-SE, as there are also unbalanced residual signals to non-intended outputs at cross/bar states configurations, the crosstalk of a 2B-SE at bar state and at cross state are measured to be -44.6 dB and -17.8 dB, respectively [6]. To resolve the issue of asymmetries, as shown in Fig. 1.2(c) 2D-SE achieves equal crosstalk (-39.7 dB) at both bar state and cross state, similar to the case in insertion loss. Albeit the asymmetric crosstalk issue are resolved, the average total crosstalks at each output-port have not been optimized and its complexity is doubled compared to that in 2B-SE in terms of number of microrings used.

1.4 Problem statement

As discussed in section 1.2, microring resonator is a very promising candidate which presents a valuable building block for photonic integrated circuits such as optical interconnection. However, the scalability of microring-based optical interconnection is limited by the following four issues which are the problems that we would like to solve in this thesis.

First, current technology for a 2×2 SE of microring requires non-negligible power consumption at cross/bar states on average [5].

Second, asymmetric loss characteristics of SEs induced high intrinsic insertion loss per path, which limits the number of successive switching elements per switching path [4,6].

Third, like the issue of insertion loss per path, the crosstalk per path also limits the

scalability of optical interconnections.

The last issue is the nonuniformity of optical power at each output-port. Due to the different insertion loss suffered by each lightpath, there is nonuniformity of output power for an optical interconnection based on 2B-SE. The difference can be significant for large interconnect size

We proposed a generic model leveraging the asymmetric behaviors of microring switching element to optimize the microring-based optical interconnection configurations for the reduction of power consumption, insertion loss, nonuniformity and crosstalk. Hence, the aim of this thesis gives a complete study of optimization of switching configurations for the reduction in overall power consumption, total insertion loss per path, non-uniformity and total crosstalk per path in a microring-based interconnection.

1.5 Motivation of this thesis

As discussed in section 1.2, though microring resonator is a promising candidate in WDM applications like optical interconnections due to its very compact footprint and sub-nanosecond switching time, microring-based optical interconnection has the scalability issue which is limited by the four issues including power consumption, insertion loss, nonuniformity and crosstalk. Indeed, there is not too much research work focusing on the optimization of the above four issues for an optical interconnection. Only two prior schemes, to be reviewed in the next chapter, were proposed to address the insertion loss issue and nonuniformity issue. These issues can be resolved by the schemes that we propose in this thesis.

In this thesis we firstly review the background of microring resonator and

microring-based optical interconnections and discuss previous work dedicated to the investigation of asymmetry and scalability issues. Severe asymmetric behaviors that limit the scalability of interconnection are also discussed to give a general background of optical interconnections. By leveraging the asymmetric characteristics at cross/bar states of microring switching elements, it is possible to achieve the optimum switching configuration for different objectives, such as the reduction in power consumption, insertion loss, nonuniformity and crosstalk. Simulation results and discussion are also presented to illustrate the optimization of power consumption, total insertion loss, nonuniformity and crosstalk per path.

1.6 Outline of this thesis

The remaining part of this thesis is organized as follows:

Chapter 2 reviews previous work on the optimization of microring-based interconnection, including the reduction in insertion loss and nonuniformity, which will be discussed in details. Additionally, relevant study on the power consumption in optical networks and the crosstalk study in optical cross connect networks will be discussed.

Chapter 3 focuses on our proposed optimization scheme of microring-based interconnection configurations for the reduction of power consumption and insertion loss. The principle to determine the optimum switching configurations, leveraging the asymmetric behaviors, will be illustrated. Calculations of the power consumption and insertion loss in optical interconnection will be shown, followed by a novel heuristic. Simulation results will also be shown and discussed in this chapter.

Chapter 4 focuses on our proposed optimization scheme of microring-based interconnection configurations for the reduction of nonuniformity and crosstalk. The principle to determine the optimum switching configurations, leveraging the

asymmetric behaviors, will be illustrated. Similar to the discussion in Chapter 3, calculations of the nonuniformity and crosstalk in optical interconnection will be shown. Simulation results will also be shown and discussed.

Chapter 2

Previous work on optimization of microring-based interconnection

2.1 Introduction

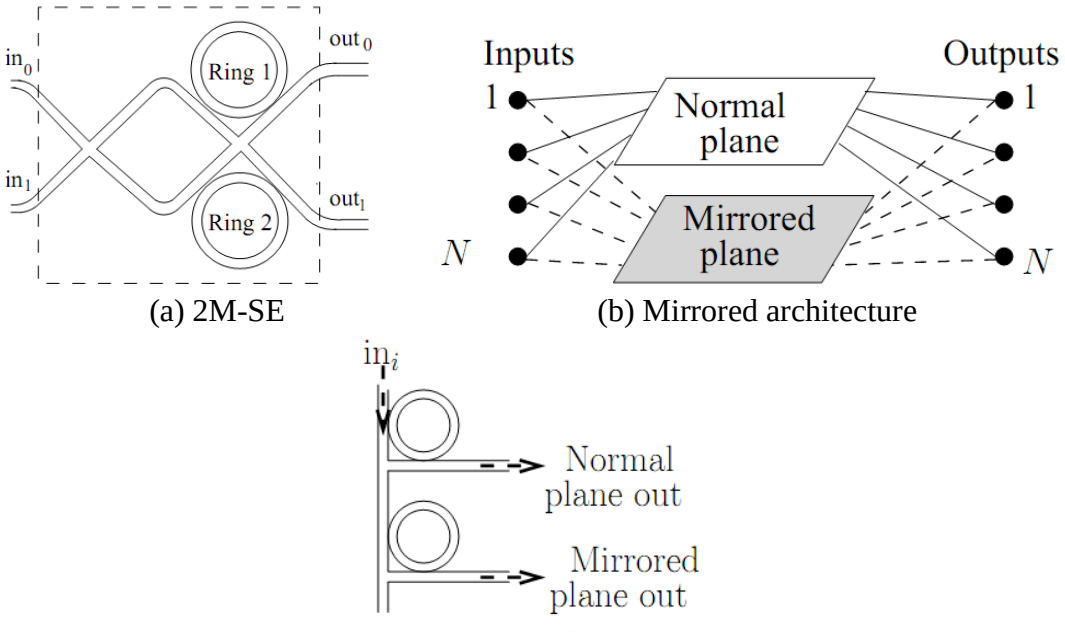
As discussed in Chapter 1, for the scalability of microring-based interconnection, the key issues, including total power consumption, insertion loss per path, nonuniformity and crosstalk per path, should be optimized. The optimizations can be achieved either by materials and physical design or by intelligent operational strategies, or by both. For microring-based interconnection, optimization by materials and physical design refers to designing a microring-based switching element with optimum characteristics, while optimization by intelligent operational strategies means that all microring-based switching elements are operated in a coordinated fashion in order to achieve the optimality. Besides, the issue of high power consumption in optical networks will be discussed and some prior work on the reduction of power consumption will be given. We will also review the study of crosstalk in optical cross connect networks.

In this chapter, we are going to review two previous schemes for addressing the issues of insertion loss and nonuniformity, respectively, in which one is by physical design and the other one is by both physical design and intelligent operational strategies. Operational principles of the two schemes will be given in details. Meanwhile, we will analyze their contributions and tradeoffs. After that, relevant study of power consumption in optical networks will be discussed.

2.2 A previous scheme for insertion loss reduction

Introduction

In order to design a basic 2×2 microring-based switching element, one can implement it with the architecture of 2B-SE as shown in Fig. 1.2(b). However, the insertion losses of 2B-SE at cross/bar states are different and thus may be accumulated to a high insertion loss per path when 2B-SE is used to build an optical interconnection. This insertion loss issue exists no matter the high insertion loss occurs at bar state or at cross state. The induced total insertion loss per path limits the scalability of an optical interconnection as the performance will be limited by the worst path.



(a) 2M-SE (b) Mirrored architecture

(c) Plane selector

Fig. 2.1. Mirroring technique [10]

2M-SE

One study optimized the insertion loss per path in multistage interconnection network by both physical design and intelligent operational strategies [10]. They proposed a new architecture for a 2×2 microring-based switching element as shown in Fig. 2.1(a) (labeled 2M-SE), which is a mirrored version of 2B-SE by

cross-connecting the input ports. As discussed in section 1.3, it can be observed that the high insertion loss occurs at bar state in 2B-SE. But in 2M-SE, the high insertion loss now occurs at cross state instead of at bar state. Leveraging this mirrored architecture, the same switching configuration of high insertion loss in 2B-SE can be realized in 2M-SE but of low insertion loss.

Mirrored plane

To improve the scalability of microring-based interconnection, a mirroring technique which exploits the spatial dimension was proposed, as shown in Fig. 2.1(b). Two different but topologically identical switching planes are used. In the normal plane, the microring-based interconnection is built with 2B-SEs only, whereas the mirrored plane is in identical topology but with 2M-SEs only. All inputs and outputs are connected to both normal and mirrored planes, in which the selector for switching planes can be a 1B-SE as shown in Fig. 1.2(a) or the plane selector depicted in Fig. 2.1(c).

Plane selector

As mentioned in section 1.3, the insertion loss of 1B-SE is 1.4 dB and 0.1 dB when the ring is in drop and through configurations, respectively. Hence, with using 1B-SE as the selector for switching planes, it introduces an additional asymmetric insertion loss (i.e., 0.1 dB and 1.4 dB) to the signals between the normal plane and the mirrored plane. This makes the layout more complex for direct connections of the drop port and the through port to their corresponding planes. Conversely, the signals to both planes via the plane selector in Fig. 2.1(c) suffer more symmetric insertion loss (i.e., 1.4 dB and 1.5 dB) due to the extra 1B-SE. This plane selector is preferable because of its simpler implementation and more symmetric insertion loss. Therefore, the plane selector was considered for the mirrored Benes interconnection in their proposed scheme.

Principle

As the normal plane and the mirrored plane are implemented by 2B-SE and 2M-SE, respectively, a switching configuration of high insertion loss in one plane will have a low insertion loss in the other plane, and vice versa. Hence, for each input-output pair, routing algorithm chooses the path along either the normal plane or the mirrored plane that gives lower total insertion loss.

Contributions and tradeoffs

By choosing the path of lower total insertion loss, the insertion loss per path of microring-based interconnection can be reduced to a certain extent. Thus the scalability issue due to the accumulated insertion loss can be resolved. However, as this scheme leverages the mirroring technique of 2B-SE to provide alternative path for same input/output pair, one mirrored plane and one plane selector are required, additionally. This scheme has a doubled complexity of that in the normal case in terms of the number of microrings, no matter the other plane is used or not. Moreover, the plane selector introduces an additional insertion loss to the signals directed to the two planes.

2.3 A previous scheme for nonuniformity reduction

Introduction

There are various possible architectures to implement a basic 2×2 microring-based switching element. 2B-SE is the simplest one but it exhibits unequal insertion loss at cross/bar state. 2M-SE is basically a mirrored version of 2B-SE and also has asymmetric insertion loss at cross/bar state. Mirroring technique with 2M-SE only addresses the scalability issue due to the high accumulated insertion loss in the worst path; it does not reduce the nonuniformity of optical power among different output-ports. As discussed in section 1.3, due to the asymmetric insertion loss at

cross/bar states, nonuniformity of optical power occurs when cascading the switching element 2B-SE or even 2M-SE to build an optical interconnection. Hence, in order to eliminate or reduce the difference between the optical power at each output-port in a microring-based optical interconnection, the insertion loss of each lightpath should be controlled to be similar or the same.

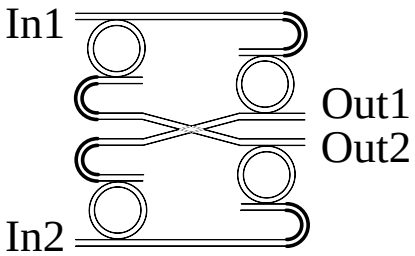


Fig. 2.2. 2D-SE

Principle: 2D-SE

One study optimized the nonuniformity of optical power at output-port in microring-based interconnection by physical design [6]. They proposed a new architecture for a 2×2 microring-based switching element as shown in Fig. 2.2 (labeled 2D-SE), which is a dilated version of 2B-SE. In 2D-SE, the incoming signals are always deflected exactly once. When a 2D-SE is configured at cross state, the incoming signal at In1 is dropped at the first microring and is directed through straightly at the second microring. This operation also holds for the incoming signal at In2. Hence, as an incoming signal always needs to pass though two microrings in cross/bar states, the total insertion loss for an incoming signal (1.5 dB) is the summation of the two losses at drop (1.4 dB) and through (0.1 dB) configurations. Different from 1B-SE and 2B-SE as discussed in section 1.3, the power penalties of 2D-SE at cross/bar state are the same. In other words, it exhibits the same insertion loss regardless of the switching configurations. Thus, when 2D-SE is used to cascade an optical interconnection, the nonuniformity of optical power is eliminated as 2D-SE does provide the same insertion loss for all possible paths.

Contributions and tradeoffs

Using the new architecture (2D-SE) to build an optical interconnection completely solves the nonuniformity issues. However, there are two drawbacks for the 2D-SE architecture. First, it exhibits double complexity in terms of the number of microrings used compared with that in the 2B-SE architecture. Second, the total insertion loss of 2D-SE at both cross and bar states is 1.5 dB, whereas in 2B-SE the insertion loss is 0.2 dB and 1.4 dB at cross and bar state, respectively. Thus, an incoming signal suffers a higher insertion loss for both cross and bar state in 2D-SE compared with that in 2B-SE. On the other hand, 2D-SE only addresses the nonuniformity issue but the total insertion loss of an optical interconnection has not been optimized.

2.4 Prior work on power consumption in optical networks

While optical network is touted as the enabling technology for future ultra-high capacity networks that can cope with the ever-increasing internet traffic, its power consumption is emerging as a challenge for network architects to balance the trade-off between large capacity and elevated carbon footprint. The Global e-Sustainability Initiative (GeSI) reported that the network infrastructures to contribute the carbon footprint of about 320 Mtons of CO_2 emissions in 2020 [11]. This estimation suggests that network switches/routers, and broadband equipments will cause carbon footprint increase by 22% and to 15%, respectively, in 2020. Other than carbon elevated footprint issues, power cost is also becoming a crucial issue. It is estimated that the total energy consumption of the network devices of a typical network service provider is about 3 TWh per year [12], which costs US$500 billion given that electricity is US$0.17/kWh. Regarding the power consumption in core network, Tucker et al. showed that the capacities and power consumptions of high-end routers grow in exponential factors of 2.5 and 1.65 every 18 months [13][14]. Hence, the power consumption has become an increasingly important issue in optical networks.

For optical interconnections, they vary in terms of switching speed, switch size (port number), electrical operating power consumption, physical footprint, as well as other properties like insertion loss, crosstalk, and reliability. Prior studies focus more on the optical performance like crosstalk, insertion loss, and faster switching speed. For large-scale optical interconnections, power consumption will be an important issue. Microring-based interconnections using thermo-optic effect needs a high power for tuning its resonance wavelength and has a low switching time in the order of microsecond [2]. Microring-based interconnections using carrier injection can achieve sub-nanosecond switching time with a lower operating power, so it has the potential for building a large integrated optical interconnection.

Solutions to the reduction of power consumption in large-scale switch fabrics could come from two origins. One category relies on innovative technologies in materials and physical design. The other category exploits intelligent operational strategies. For example, a study on power-efficient interconnection networks uses dynamic voltage scaling with links [15], in which the frequency and voltage of links are dynamically adjusted based on past link utilization in order to optimize the power consumption. Although this approach realizes 3.2 times power saving on average, it introduces an increase of 27.4% latency and a reduction of 2.5% throughput. It also requires sophisticated hardware for fast, online voltage and frequency changes. One study on hybrid optical switches using two switching technology is proposed [16], Hybrid switches comprising 3D-microelectonic mechanical systems (MEMS) switches and conventional electronic packet switches, and 3D-MEMS switches and semiconductor optical amplifier (SOA)-based switches, are studied. It showed the power consumption increases with the ratio of fast to slow traffic. Energy efficiency is improved in both cases, compared with switches using single switching technology.

On the power-aware design and routing in optical networks, there are several studies discussing the model of power consumption in IP networks. A broad approach to

cope with the power consumption issues of routes by network design, configuration and protocols are discussed in [17]. A general model for power consumption of routers is developed using the measured figures of various configurations of chassis types and line cards in routers. One study of the energy-awareness in backbone networks is investigated in [18]. They propose an algorithm to select the network components to be powered-down during low-traffic period without loss of the service guarantee. A power-aware scheme using traffic engineering approach for minimizing the operational power in optical backbone networks is proposed [19]. The power efficiency of two green strategies, optical bypass and traffic grooming, are analyzed by evaluating the constituent power consumption. One comprehensive paper about the energy consumption in fixed broadband networks, mobile radio networks and data centers is investigated in [20]. Different metrics for energy/power efficiency are also discussed in the paper, including overall energy/power consumption, energy/power per bit of data, and Power Usage Effectiveness (PUE) ratio for data centers. In the model, using the power consumption values and operation time of network elements, they estimated the energy consumption by considering the predicted traffic volume, subscriber developments and network elements developments as well as the timeframe.

The prior research on power consumption in optical networks aims at minimizing the power consumption by means of traffic grooming, re-routing or powering-off unused devices or interfaces. Alternative paths that give lower power consumption can be identified by these approaches. The principle of reducing the power consumption is similar in optical interconnections. Thus, the prior work on power consumption in optical networks may be applicable to optical interconnection.

2.5 Prior work on crosstalk in optical cross-connect networks

The study of crosstalk in microring-based interconnections is similar to the study of

crosstalk in optical cross-connect (OXC) networks. There are several schemes proposed to evaluate the limit of the number of node and the node size for scalability study [21-23]. However, switching architectures of OXC are ignored during the calculation in prior studies. Crosstalk accumulation not only depends on single component performance, but also depends on the network performances. Thus, OXC architectures should be carefully adopted and designed to minimize crosstalk and relax the scalability restrictions [24-26].

One prior work investigated the influence of crosstalk on the scalability of WDM cross-connect networks [27]. In their work, the crosstalk contributions of different components including MUXs, DEMUXs and optical switches in OXC are studied. Three different node topologies based on Benes architectures are studied. Only the first- and second-order crosstalk contributions are considered whereas higher-order crosstalk contributions are ignored. Results revealed that the first-order crosstalk contributions are dominated by the crosstalk from the switch fabric. The results indicate that increasing the number of wavelengths is much better than increasing the number of fabrics when the node size needs to be increased.

2.7 Summary

We have reviewed two prior schemes for resolving the problems of nonuniformity and insertion loss, respectively. One scheme is by physical design and the other one is by both physical design and intelligent operational strategies. For the insertion loss issue, the scheme of mirroring techniques with 2M-SE architectures and a plane selector effectively reduces the insertion loss per path at the expense of doubling the number of microrings used. For the nonuniformity issue, the scheme using 2D-SE to build an optical interconnection gives uniform optical power at output-ports, but with the tradeoff of higher insertion loss at cross/bar states and doubled complexity in terms of the number of microrings used, compared with that in 2B-SE. We have also

discussed the issue of the high power consumption in optical networks and presented some prior schemes to address the problem. Finally, several prior work on crosstalk study in OXC networks are reviewed.

From the next chapter, we will start to discuss our proposed scheme to achieve the optimum switching configuration for different objectives that include the reduction in power consumption, insertion loss, nonuniformity and crosstalk, by leveraging the asymmetric characteristics at cross/bar states of microring switching elements.

Chapter 3
Optimization scheme of microring-based interconnection configurations for reduction of power consumption and insertion loss

3.1 Introduction

As discussed in section 1.4, microring resonator is a very promising candidate to be a valuable building block for optical interconnection. However, the scalability of microring-based optical interconnection is limited by the aforementioned four issues that we would like to resolve in this thesis. In Chapter 2, we have reviewed two prior schemes that address the problems of high accumulated total insertion loss per path and the nonuniformity of optical power among different output-ports in a microring-based optical interconnection. In Chapter 3 and Chapter 4, we will study the scalability problem in a more comprehensive way and provide our proposed scheme to resolve the four problems.

In this chapter, we will focus on the first two issues: (1) reduction of power consumption of microring-based optical interconnection using 2×2 SEs; (2) reduction of high accumulated total intrinsic insertion loss per path due to unequal loss characteristics of SEs. With the objectives of minimizing the overall power

consumption and total insertion loss per path of a microring-based interconnection, our proposed scheme is able to determine the optimum switching configurations by leveraging the asymmetric behaviors of the switching element. In addition, calculations of the total power consumption and the total insertion loss per path in an optical interconnection will be shown, followed by a novel heuristic. After that, simulation results will be shown and discussed. Finally, we will give a summary of the proposed scheme.

3.2 Principle of determining the optimum switching configurations

The following describes a generic principle in determining the optimum switching configurations for total power consumption and average total insertion loss per path of classical switch architectures. A large-scale microring-based optical interconnection which is constructed by cascading N number of 2B-SEs (a 2×2 switch) will be examined. In an $n \times n$ switch, there are 2^N sets of switching configurations to satisfy $n!$ possible traffic matrices. For each traffic matrix, T, there may be more than one possible configuration as $2^N > n!$.

Fig. 3.1. Abstract of a 4×4 Benes switch

A 4×4 Benes switch is selected as an example for illustration since it exhibits minimum complexity among various nonblocking architectures. As shown in Fig. 3.1, a 4×4 Benes switch can be viewed as a black box which is composed of 2×2 switching elements only. For the given input/output pairs, we can always find the corresponding traffic matrices. Fig. 3.2 shows an example of traffic-demand

transformation for transforming input/output pairs request to a traffic matrix, T_0.

Input	1	2	3	4
Output	3’	4’	2’	1’

$$\Rightarrow \qquad T_0 = \begin{pmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix}$$

(a) Input/output pairs request (b) Traffic matrix

Fig. 3.2. Traffic-demand transformation

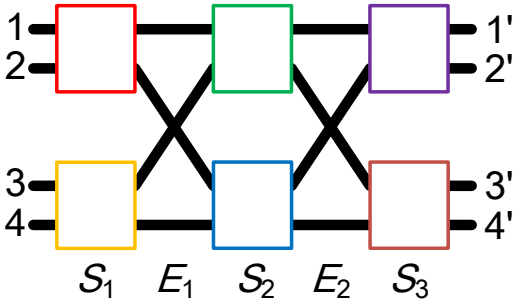


Fig. 3.3. 4×4 Benes interconnection using 2×2 switching elements

The above interconnection can be expressed as $T=S_3\times E_2\times S_2\times E_1\times S_1$ which is equal to the following Eq. 3.1. It should be noted that there is one 2B-SE in each color block.

$$T = \begin{pmatrix} s_{31} & s'_{31} & 0 & 0 \\ s'_{31} & s_{31} & 0 & 0 \\ 0 & 0 & s_{32} & s'_{32} \\ 0 & 0 & s'_{32} & s_{32} \end{pmatrix} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} s_{21} & s'_{21} & 0 & 0 \\ s'_{21} & s_{21} & 0 & 0 \\ 0 & 0 & s_{22} & s'_{22} \\ 0 & 0 & s'_{22} & s_{22} \end{pmatrix} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} s_{11} & s'_{11} & 0 & 0 \\ s'_{11} & s_{11} & 0 & 0 \\ 0 & 0 & s_{12} & s'_{12} \\ 0 & 0 & s'_{12} & s_{12} \end{pmatrix}$$

Eq. 3.1. Interconnection representation

The interconnection representation in Eq. 3.1 shows a generic decomposition of an interconnection based on 2×2 switching elements. There are many possible switching configurations for achieving the same traffic matrix T. All possible configurations can be found by the equation of $T=S_3\times E_2\times S_2\times E_1\times S_1$. The variables S_1, S_2 and S_3 are stage matrices, consisting of the switching configurations of the 2B-SEs at the first, second and third stage, respectively, where E_1 and E_2 are edge matrices for the interconnection between each stage. Hence, T can be expressed as Eq. 3.1. s_{ij} and s_{ij}’ represent the bar/cross state of the j^{th} 2B-SE (represented by different color blocks in

Fig. 3.3 and Eq. 3.1) at stage-i, where $s_{ij} = 1$ (0) denotes the switch is at bar (cross) state. It should be noted that s_{ij} and s_{ij}' are binary and complementary of each other.

First, for the given input/output pairs in Fig. 3.2(a), we can obtain the traffic matrix T_0 as in Fig. 3.2(b). By analyzing T_0 using Eq. 3.1, we can find all possible switching configurations. There are four possible configurations after solving the equation for the T_0 in Fig. 3.2(b). Different configurations, depending on the number of cross/bar states, result in different total power consumption as well as different total insertion loss per path. Fig. 3.4(a)-(d) depict all four possible switching configurations for the given T_0 and the corresponding number of bar-state and cross-state switches.

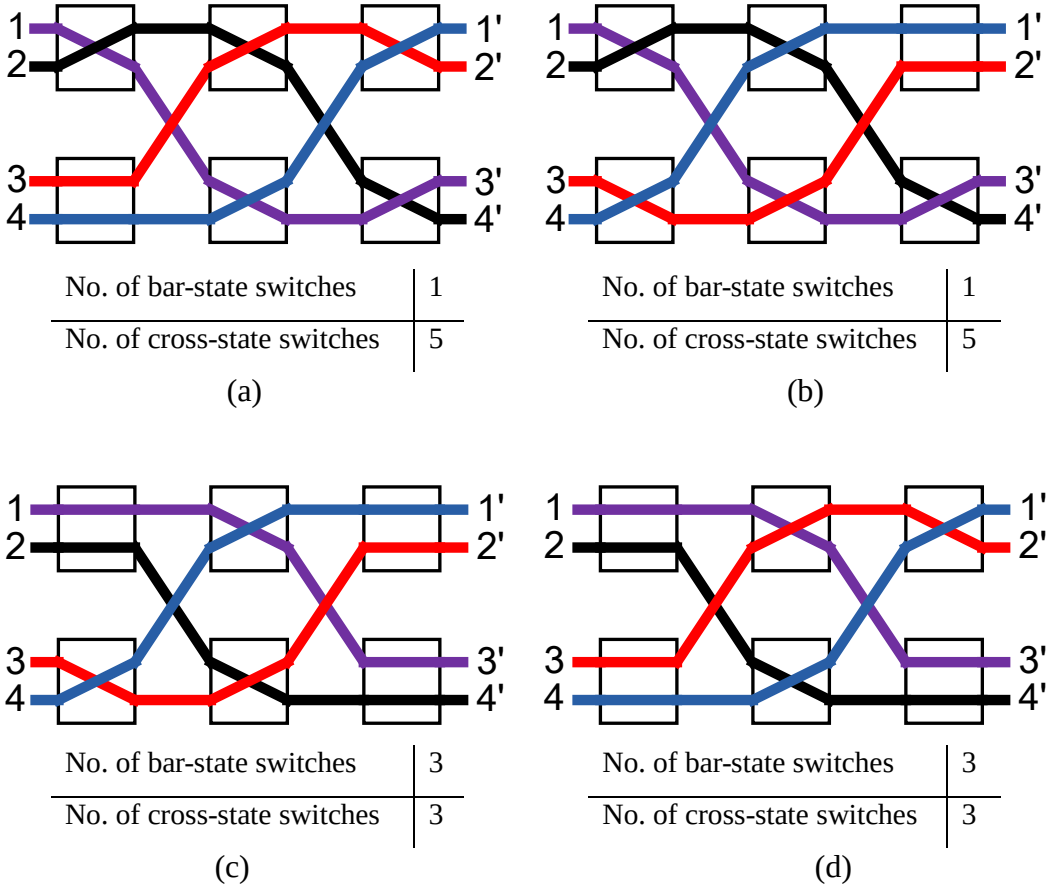


Fig. 3.4. (a)-(d) Possible switching configurations for traffic matrix T_0

We first take the minimization of total power consumption as the objective function. The same principle holds for the reduction of total insertion loss per path. The operating power for a 2B-SE at bar state, P_b, is assumed to be higher than that at

cross state, P_c, without loss of generality. The two configurations in Fig. 3.4(a) and (b) are the optimum switching configurations of total power consumption = P_b+5P_c, whereas the other two in (c) and (d) are of high total power consumption, 3P_b+3P_c.

When the number of ports increases, the above equations are still valid by multiplying more stage matrices and edge matrices. Hence, the total power consumption of an $n \times n$ Benes switch can be optimized by configuring the 2B-SEs appropriately. In simulations, we generated 2^N sets of configurations up to 100,000 sets for a large value of N to match certain traffic matrix, in which the switching configuration with the minimum total number of bar-state switches will be selected as the optimum switching configuration. The average number of bar state switches for an $n \times n$ switch is the average number of bar-state switches of the optimum configuration for each traffic matrix.

3.2.1 Calculations of power consumption and insertion loss

Without loss of generality, we assume the following parameters for 2B-SE in our study: (1) the power consumption at bar state (P_b) and cross state (P_c) are 200 μW and 0 μW, respectively; (2) the insertion loss at bar state (IL_b) and cross state (IL_c) are 1.4 dB and 0.2 dB , respectively.

The principle of determining the optimum switching configuration for the reduction of total power consumption is discussed in the previous section. With the objective of the reduction of total insertion loss per path in 2B-SEs, we apply the same principle as in the power consumption case. If the bar-state switch has higher power consumption and higher insertion loss, the two objectives of the reduction of the overall power consumption and the average total insertion loss per path can be achieved simultaneously by minimizing the total number of bar-state switches which is:

$$\sum_{i,j} s_{i,j} \qquad \text{Eq. 3.2}$$

The objective functions for minimizing the total power consumption, P_T, and the average total insertion loss per path, IL_T, are to minimize the total number of bar state switches. Therefore, the objective function for the minimization of the total power consumption is:

$$\min_{s_{ij}, s'_{ij} \in \{0,1\}} \left\{ P_b \sum_{i,j} s_{i,j} + P_c \sum_{i,j} s'_{i,j} \right\} \qquad \text{Eq. 3.3}$$

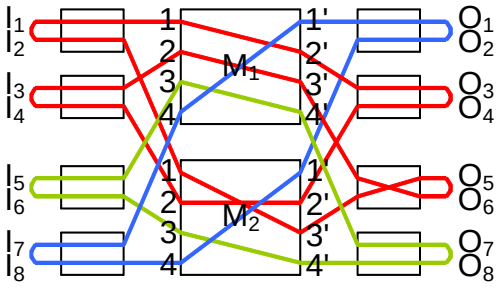
Similarly, the objective function for the minimization of the average total insertion loss per path is:

$$\min_{s_{ij}, s'_{ij} \in \{0,1\}} \left\{ [IL_b \sum_{i,j} s_{i,j} + IL_c \sum_{i,j} s'_{i,j}] / n \right\} \qquad \text{Eq. 3.4}$$

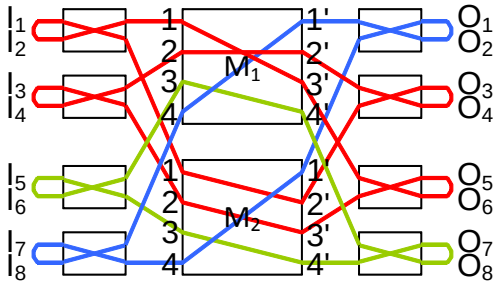
It should be noted that the scheme proposed is also applicable for classical switch architectures.

3.3 Heuristic for reduction of power consumption and insertion loss

To find the optimum switching configuration with shorter computation time, we develop a novel heuristic to minimize the number of bar-state switches (i.e. changed to the switching configuration of lower insertion loss or lower power consumption). For Benes architecture, it presents an iterative procedure for changing bar state to cross state recursively for each loop. Fig. 3.5 shows the switching configuration optimization by the looping algorithm. The procedure is illustrated as follows:



(a) Switching configuration before optimization



(b) Optimum switching configuration for outer stages

Fig. 3.5. Switching configuration optimization by the looping algorithm

Step 1

For a given initial configuration, the inputs and outputs are connected by the looping algorithm as shown in Fig. 3.5(a). 2×2 SEs at the first and third stage in different loops are independent in changing states. (Looping algorithm in Benes architecture is used to setup a matching request for input/output pairs to identify all the states of SEs.)

Step 2

For each loop, all SEs at the first stage (e.g. SE of port I_1 and I_2; SE of port I_3 and I_4) and the third stage (e.g. SE of port O_3 and O_4; SE of port O_5 and O_6) are changed to their opposite states at the same time if there are more bar-state SEs in that loop. Otherwise, the change of configuration for SEs at the first and third stage is finished.

Step 3

As shown in Fig. 3.5(a), if the loop passes through two central modules (M_1 & M_2), input-output pairs in the same loop at M_1 (ports in M_1: 1→2'; 2→3') will interchange input-output pairs in the same loop at M_2 (ports in $M_{2:}$ 1→3'; 2→2'). Fig. 3.5(b) shows the switching configuration after changing bar state to cross state.

Step 4

An $n \times n$ Benes switch can be decomposed into two $N/2 \times N/2$ modules in the middle consisting of 2×2 SEs at the first and third stage. An $N/2 \times N/2$ module can then be broken down into three stages consisting of 2×2 SEs at the first and third stage and repeat from ***step 1***. The change is performed recursively from the outer stages to the inner stages until the central module becomes 2×2 SEs.

After the heuristic, the number of bar-state switches is minimized and thus the optimum switching configurations for the minimization of the total power consumption and the average total insertion loss per path are achieved.

The computation time of determining the optimum switching configurations using the heuristic is analyzed, compared with that using exhaustive search. Fig. 3.6 shows that our heuristic can reduce the computation time to one third of the exhaustive search. The improvement using the heuristic is substantial at a larger switch size. Hence, it demonstrates that the proposed heuristic for finding the optimum switching configuration is efficient.

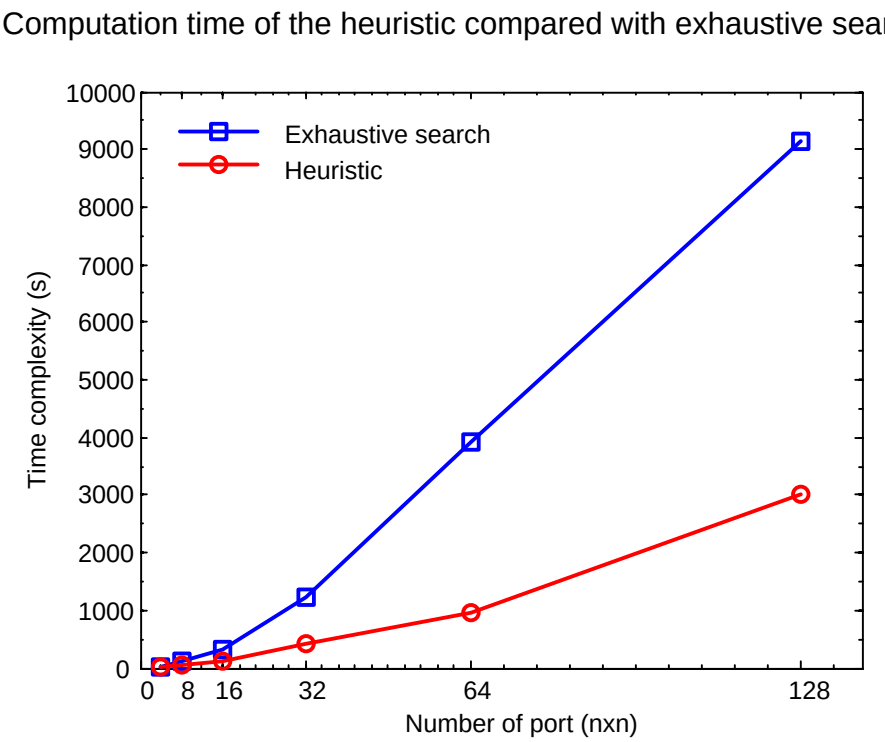


Fig. 3.6. Computation time of the heuristic compared with exhaustive search

3.4 Simulation results and discussion

Power consumption

Using the measurement values as mentioned in section 1.3, the power saving using the optimum switching configuration for a given switch size is obtained and compared with the average power consumption without optimization. The results in Fig. 3.7 show that significant power savings for Benes, Spanke-Benes and Crossbar switch [28] can be achieved for a 128×128 switch. The curve shows that the power saving of the optimum switching configuration increases with the number of ports. Crossbar switch has the best performance due to its high flexibility. Benes network exhibits the minimum complexity (rearrangeably nonblocking), measured in number of switch elements. Instead, Spanke-Benes network has more number of switch elements than Benes network, but at similar blocking probability (rearrangeably nonblocking) as Benes network. For Crossbar network, it has the lowest blocking probability (wide-sense nonblocking) with the largest number of switch elements. As

Crossbar switch exhibits the lowest non-blocking probability among the three architectures, it has more number of possible switching configurations to satisfy a given traffic matrix. Thus, the power saving is the highest among the three architectures.

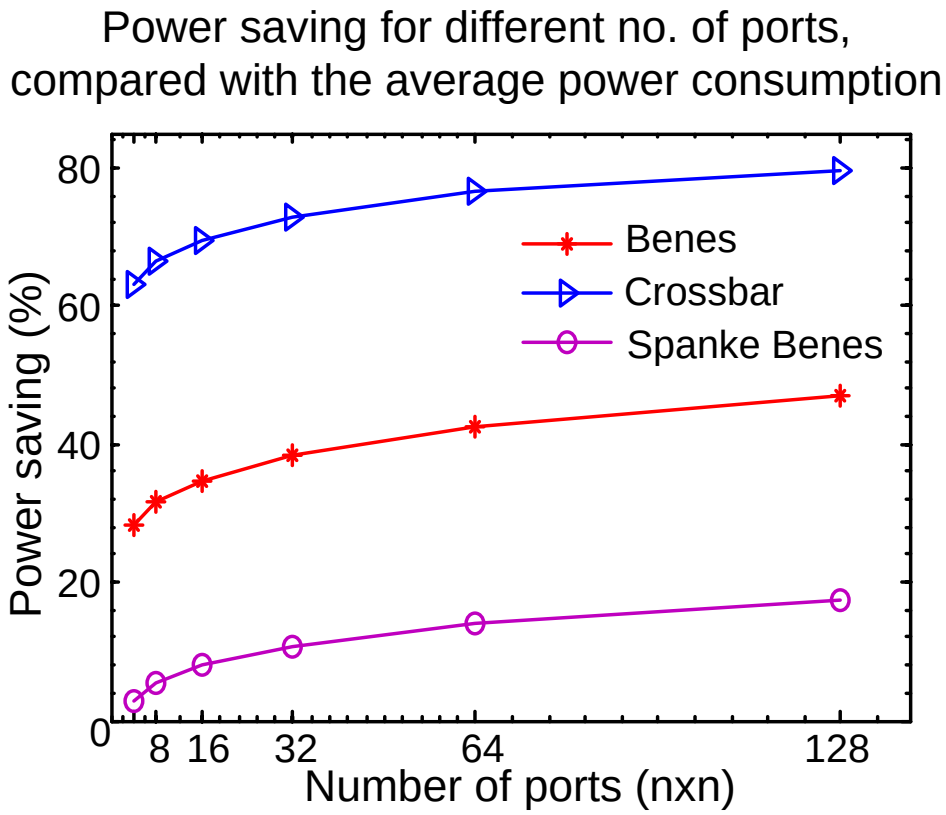


Fig. 3.7. Simulation results of the power saving for different number of ports

Fig. 3.8 depicts the absolute power consumption for different switch architectures. It increases nonlinearly with the number of ports. Albeit Crossbar switch achieves a high power saving, its absolute power consumption is almost double of that for Benes switch for 128×128 switch size due to the high complexity of Crossbar switch.

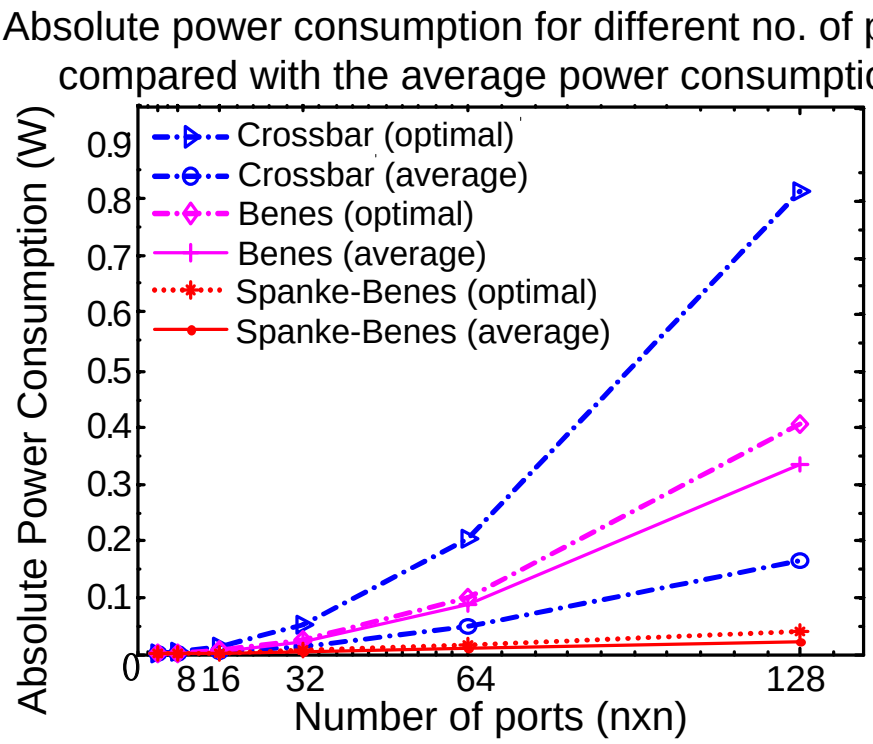


Fig. 3.8. Simulation results of the absolute power consumption for different switch architectures for different number of ports

We further investigate the effect of symmetry in cross/bar state on the relative power saving. R is defined as $R=P_c/P_b$. We denote C to be the sum of P_c and P_b, $C=P_c+P_b$. P_c and P_b can be written as $P_c=CR/(1+R)$ and $P_b=C/(1+R)$, respectively. Without optimization, since each traffic demand is equally probable, the numbers of bar-sate switches and cross-state switches both equal to $N/2$ on average. Hence, the total power consumption before and after optimization are $P_{T\_org}=C(N/2+N/2)/2=CN/2$ and $P_{T\_opt}=P_c(N-N_{b\_opt})+P_bN_{b\_opt}$, respectively, where N_{b_opt} is the minimum total number of bar-state switches using the optimum configuration. The relative power saving, r is then simplified as:

$$r=\frac{P_{T\_org}-P_{T\_opt}}{P_{T\_org}}=1-\left[\frac{R}{1+R}\right]\left[2-\frac{2N_b}{N}\right]-\left[\frac{1}{1+R}\right]\left[\frac{2N_b}{N}\right] \qquad \text{Eq. 3.5}$$

It is observed that the relative power saving depends on the degree of power symmetry, R, and the ratio of switch in bar state, N_b/N. Thus, optical interconnections with the same R in SEs achieve the same relative power saving regardless of the absolute power consumption for each SE.

Fig. 3.9 shows the results of power saving for different degree of power symmetry. Results reveal that the higher the degree of power symmetry, the lower the power saving. Power saving attains its maximum when P_c=0. In other words, it is favorable to fabricate a microring SE with higher asymmetry in power consumption at cross/bar states for lower overall power consumption, assuming the total power consumption of bar- and cross-state is constant.

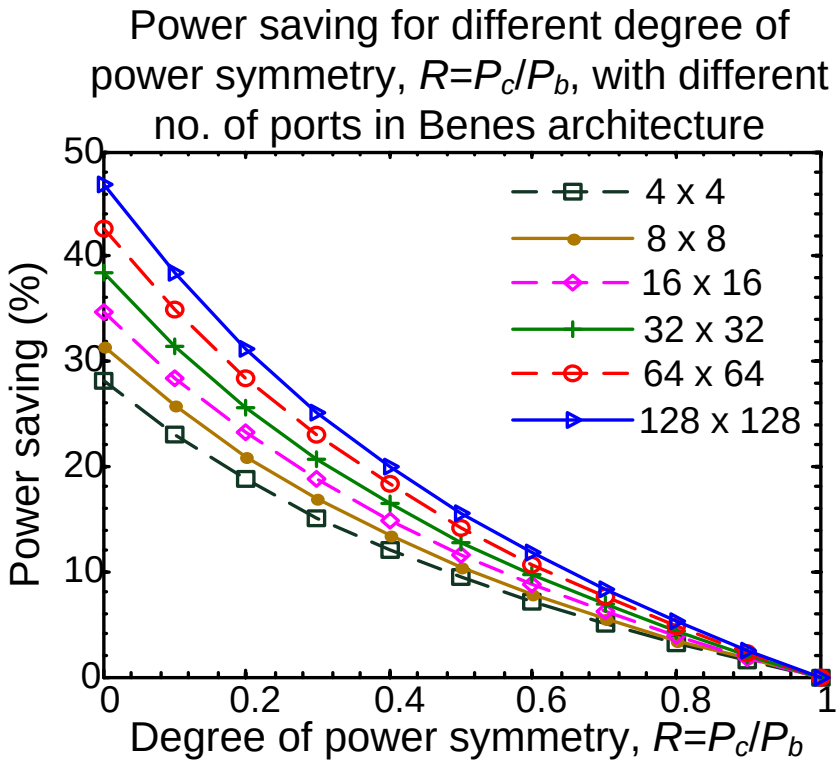


Fig. 3.9. Simulation results of the absolute power consumption for different switch architectures for different number of ports

Insertion loss

On the other hand, the total insertion loss per path is a dominant factor for the scalability of optical interconnections. Simulations are performed to minimize (1) the average total insertion loss per path and (2) the insertion loss of the worst path. Fig. 3.10 shows that the average total insertion loss per path increases with the number of ports in Benes architecture. The average total insertion loss per path using 2B-SEs achieves a 3.65-dB improvement while the optimum average total insertion loss using 2B-SEs in worst-case path (WCP) has a 7.2-dB improvement for 128×128 switch size at optimum switching configurations compared with the baseline values without optimization. There is no optimization for the microring-based interconnection using 2D-SEs because it attains the same insertion loss at cross/bar states.

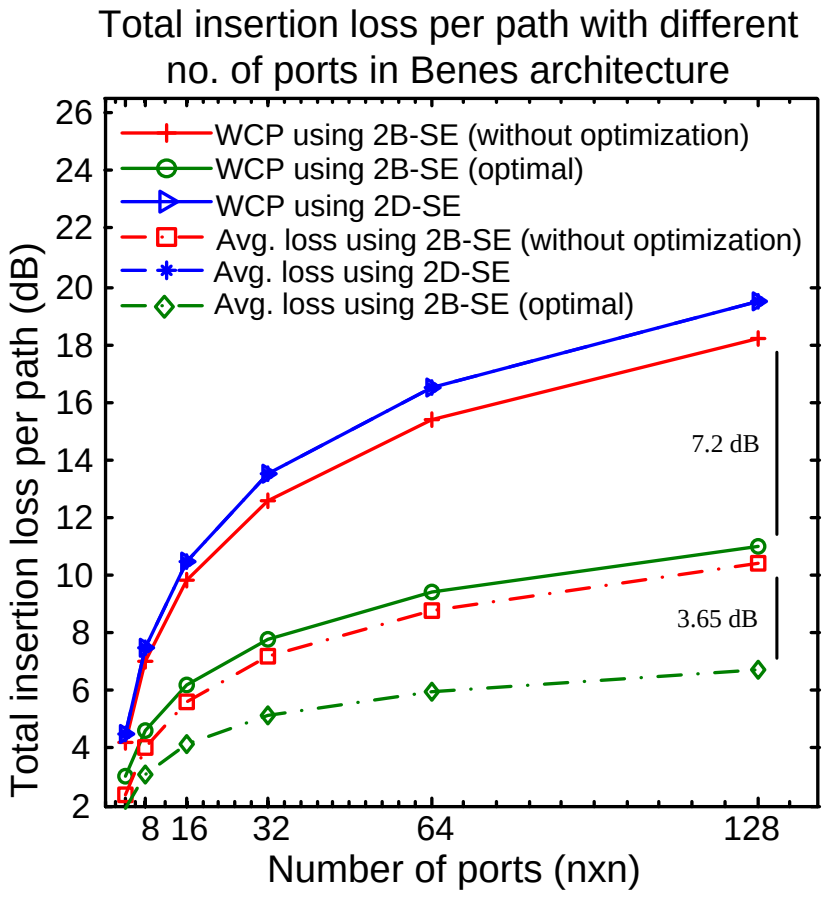


Fig. 3.10. Total insertion loss per path with different number of ports in Benes architecture

3.5 Summary

In this chapter, we successfully demonstrated that with the optimum switching configuration, the overall power consumption, the average total insertion loss per path as well as the insertion loss of the worst-case path can be reduced for microring-based interconnections. A novel heuristic is proposed to reduce the computation time for the optimum switching configuration. The results also show that the optimum average total insertion loss per path using 2B-SE achieves a 3.65-dB improvement for 128×128 switch size. The optimum average total insertion loss using 2B-SE in the worst-cast path is shown to be 7.2 dB less than the baseline value without optimization.

Chapter 4

Optimization scheme of microring-based interconnection configurations for the reduction of nonuniformity and crosstalk

4.1 Introduction

Besides the problems of the total power consumption and the total insertion loss per path, nonuniformity of optical power among different output-ports and the total crosstalk at each output-port are also the factors limiting the scalability of microring-based interconnections as discussed in section 1.3. In Chapter 2, the scheme of resolving the nonuniformity problem by the mirroring technique is reviewed. In Chapter 3, we have discussed our proposed scheme to minimize the total power consumption and the total insertion loss per path. Thus, in this chapter we will focus on the remaining problems: (1) the nonuniformity of optical power among different output-ports and (2) the total crosstalk at each output-port.

As mentioned in section 1.3, the optical power among different output-ports of an optical interconnection may be different due to the unequal insertion loss at cross/bar states of 2B-SE. This will result in the nonuniformity of optical power, thus limiting the scalability of an optical interconnection. As the nonuniformity of optical power depends on the total insertion loss per path, the scheme to minimize the nonuniformity requires the calculation of the total insertion loss per path. However, the objective function is different from the minimization of the total insertion loss per path as shown in the previous chapter.

On the other hand, there is non-intended power leakage, the crosstalk, to the non-destined output in 2B-SE at both cross- and bar-states. Crosstalk limits the number of successive switching elements per switching path. When 2B-SE is used to build an optical interconnection, there will be many possible crosstalk powers going to the same output-port. We are going to present and discuss our proposed scheme for reducing the total crosstalk power at each output-port.

With the objectives of minimizing the nonuniformity of optical power among different output-ports and the total crosstalk at each output-port of a microring-based interconnection, we propose an optimization scheme to determine the optimum switching configurations. In addition, calculations of the nonuniformity and the crosstalk power in an optical interconnection will be shown in details. After that, simulation results will also be given and discussed. Finally, we will give a summary of this scheme.

4.2 Principle of determining the optimum switching configurations

The following describes a generic principle in determining the optimum switching configurations for nonuniformity of optical power and total crosstalk at each output-port of classical switch architectures. The interconnection representation of a microring-based optical interconnection is the same as we discussed in Chapter 3. By applying the principle for identifying all the possible switching configurations for a given input/output pairs, we can always find the corresponding traffic matrix as well as all possible switching configurations. Different configurations, depending on the number of cross/bar-states that each path passes through, result in different nonuniformity of optical power among all output-ports as well as different total crosstalk at each output.

A 4×4 Benes switch composed of 2×2 switching elements is selected as an example for illustration. First, for a given input/output pairs, T_0 in Fig. 4.1(b) is analyzed. All possible switching configurations can be found as depicted in Fig. 4.2(a)-(d).

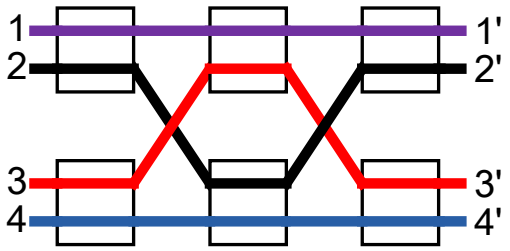
Input	1	2	3	4
Output	1’	2’	3’	4’

(a) Input/output pairs request

$$T_0 = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix}$$

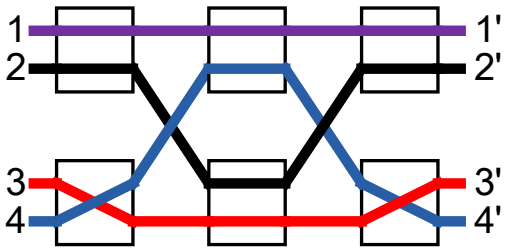
(b) Traffic matrix

Fig. 4.1. Traffic-demand transformation



Output-port	1’	2’	3’	4’
No. of bar-state switches	3	3	3	3
No. of cross-state switches	0	0	0	0

(a)



Output-port	1’	2’	3’	4’
No. of bar state switches	3	3	1	1
No. of cross state switches	0	0	2	2

(b)

Output-port	1’	2’	3’	4’
No. of bar state-switches	1	1	3	3
No. of cross-state switches	2	2	0	0

(c)

Output-port	1’	2’	3’	4’
No. of bar-state switches	1	1	1	1
No. of cross-state switches	2	2	2	2

(d)

Fig. 4.2. (a)-(d) Possible switching configurations for traffic matrix T_0

4.2.1 Calculation of nonuniformity

We first take the minimization of nonuniformity of optical power among different output-ports as the objective function. The insertion loss for a 2B-SE at bar-state, IL_b, is assumed to be higher than that at cross-state, IL_c, without loss of generality. The two configurations in Fig. 4.2(a) and (d) are the optimum switching configurations with no nonuniformity (uniform power), whereas the other two in (b) and (c) are of high nonuniformity (=$2IL_b$-$2IL_c$). It should be noted that the nonuniformity of optical

power among different output-ports is calculated by the difference between the largest optical output power and the smallest optical output power among all output-ports.

When the number of ports increases, the above calculations are still valid by multiplying more stage matrices and edge matrices. Hence, the total power consumption of an $n \times n$ Benes switch can be optimized by configuring the 2B-SEs appropriately. The switching configuration with the lowest nonuniformity of optical power among different output-ports will be selected as the optimum switching configuration. It should be noted that the scheme proposed is also applicable for classical switch architectures.

4.2.2 Calculation of crosstalk

With the minimization of the total crosstalk at each output-port being the objective function, we first find all possible switching configurations for a given traffic matrix T_0. After identifying all possible switching configurations as in Fig. 4.2(a)-(d), we need to determine the optimum switching configuration that gives the smallest total crosstalk at each output-port on average. The crosstalk for a 2B-SE at cross-state is assumed to be higher than that at bar-state without loss of generality.

The switching configuration in Fig. 4.2(a) is taken as an example to illustrate the calculation of the total crosstalk at each output-port. For better understanding, we re-draw the switching configuration in Fig. 4.2(a) as shown in Fig. 4.3. Crosstalk power and signal power are marked as dotted line and thick line, respectively.

In this three-stage Benes interconnection, there are first-order, second-order and third-order crosstalks. The highest number of order is the same as the number of stages for an S-stage Benes interconnection. The number of n-order crosstalks destined to each output-port in S-stages Benes interconnection is ${}_S\mathrm{C}_n$. Hence, for each

output-port, there are three 1st-order, three 2nd-order and one 3rd-order crosstalks in this 3-stage Benes interconnection. The calculation of the total crosstalk of each path is shown as follows.

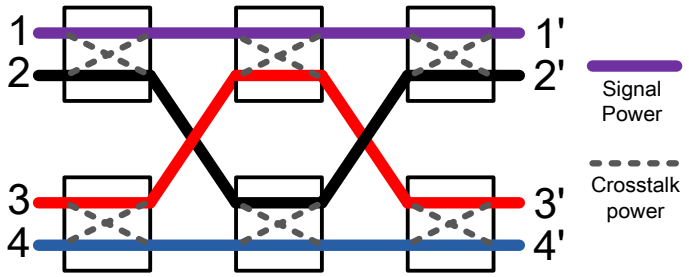
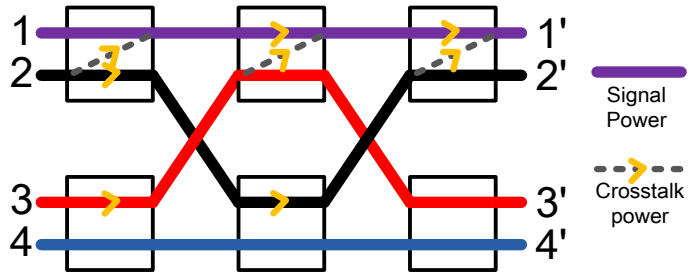
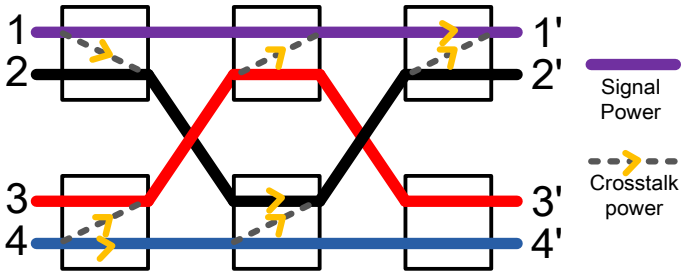


Fig. 4.3. One possible switching configuration for traffic matrix T_0 showing signal and crosstalk power

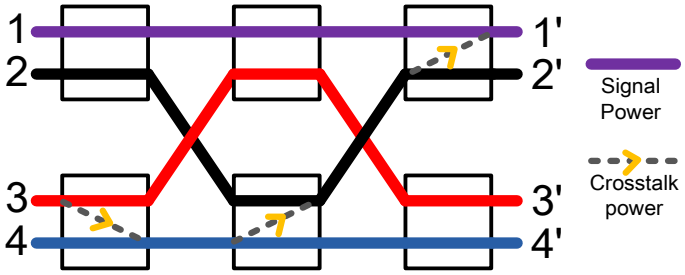
For each output-port, the calculation of the total crosstalk is similar. The total crosstalk at output-port 1' is contributed by the first-order, second-order and third-order crosstalks as shown in Fig. 4.4(a), (b), and (c), respectively. After determining all the total crosstalk at each output-port, we take the average value as well as the maximum value among all the output-ports. As different switching configurations result in different total crosstalk at each output-port, the switching configuration that gives the smallest total crosstalk is chosen as the optimum switching configuration.



(a) Three 1st-order crosstalks destined to output-port 1'



(b) Three 2nd-order crosstalks destined to output-port 1'



(c) One 3rd-order crosstalk paths destined to output-port 1'

Fig. 4.4. Contributions of different order crosstalks to output-port 1'

For a large-scale interconnection, it is envisioned that the number of crosstalks and the highest crosstalk order increases with the switch size as the number of possible crosstalk paths from each output-port and the number of switch stage increases. In Fig. 4.5, the upper bound of the n^{th}-order crosstalk is estimated by selecting the path with the highest crosstalk among all n^{th}-order crosstalk paths. For each switch size, the crosstalk contribution for each crosstalk order decreases when the crosstalk order increases. For a given crosstalk order, the amount of crosstalk increases with the switch size. It shows that the contributions of those higher-order crosstalks are insignificant compared with the lower-order terms. In our simulations, only the contributions of the first three order crosstalks are considered as the 4^{th}-order term is less than -40 dB for switch size up to 128×128.

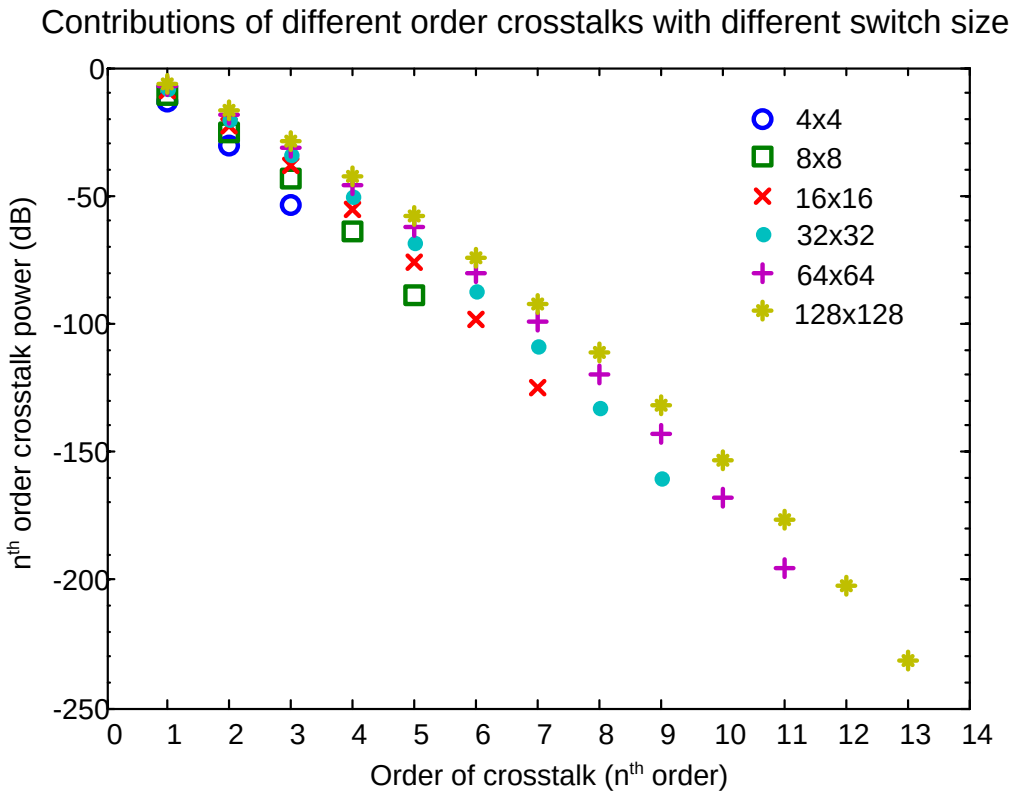


Fig. 4.5. Contributions of different order crosstalks with different switch size

4.3 Simulation results and discussion

Nonuniformity

Using the measurement values as mentioned in section 1.3, we first calculate the value of the total insertion loss per path at each output-port and then obtain the nonuniformity of optical power among different output-ports. The nonuniformity of optical power under the optimum switching configuration for a given switch size is obtained. Simulation results are shown in Fig. 4.6. In our simulations, we have investigated several nonuniformity cases. The maximum nonuniformity corresponds to the worst case in which the switching configuration gives the highest nonuniformity for a given traffic matrix whereas the minimum nonuniformity corresponds to the optimum switching configuration. The average nonuniformity corresponds to the average nonuniformity among all switching configurations in one switch size without optimization. The average of optimum nonuniformity and the

average of the maximum nonuniformity for all traffic matrices increase with the number of switch size as shown in Fig. 4.6. The optimum nonuniformity for 128×128 switch size has a 3.21-dB improvement on average, compared with the average nonuniformity without optimization.

For each traffic matrix, the worst case corresponds to the switching configuration that gives the maximum nonuniformity. Besides studying the average of the nonuniformity of worst cases among all traffic matrices at one particular switch size, we also investigate the maximum nonuniformity among all traffic matrices (i.e., the worst case of the worst case, labeled as WWC). However, among different traffic matrices at one particular switch size, WWC may not be unique as the nonuniformity of their worst case could be the same before optimization. But they may have different improvements after optimization. Hence we investigate the minimization of the nonuniformity among WWCs using the optimum switching configuration and identify the best improvement (i.e., minimum nonuniformity of WWC), average improvement (i.e., average nonuniformity of WWC) and the least improvement (i.e., maximum uniformity of WWC) using the optimum switching configurations. Results show that in WWC, it can achieve significant improvement. With the optimum switching configuration, the best improvement is 9.6 dB, the average improvement is 8.7 dB and the least improvement is 7.2 dB for 128×128 switch size. It should be noted that the nonuniformity of optical power among different output-ports is linearly proportional to the difference between the insertion loss at bar-state and that at cross-state.

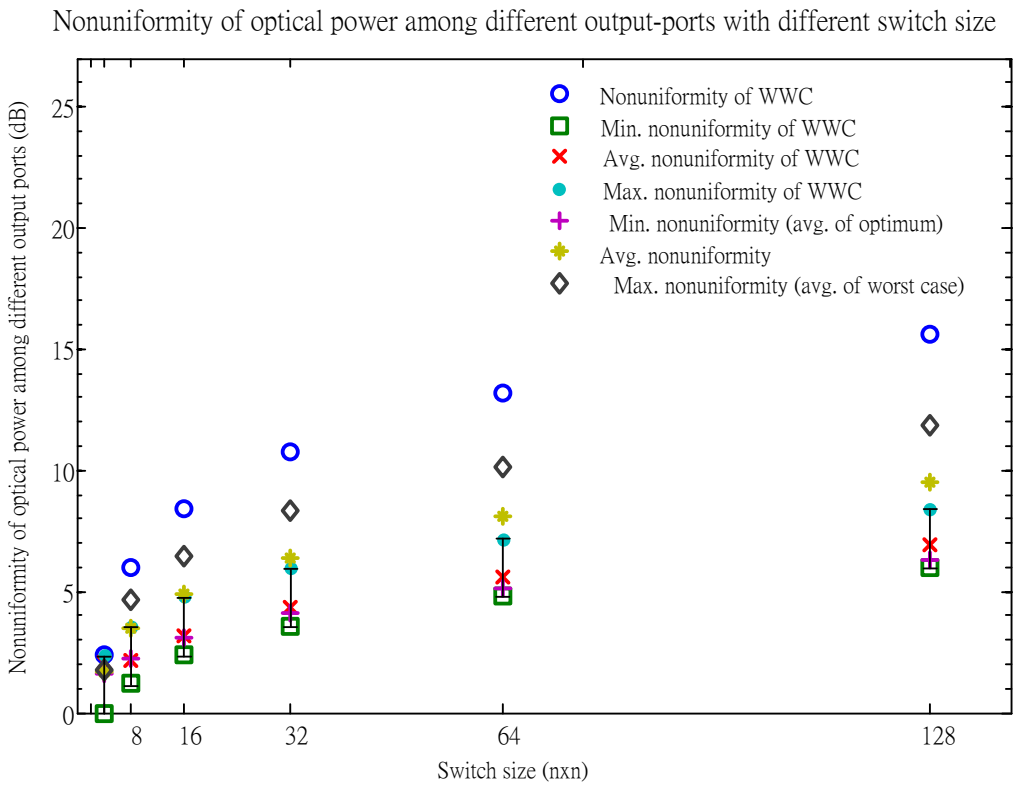


Fig. 4.6. Nonuniformity of optical power among different output-ports with different switch size

Crosstalk

Besides the nonuniformity, the total crosstalks at each output-port with the optimum switching configuration for different switch size are investigated. Results depicted in Fig. 4.7 show that the optimum switching configuration can achieve a 1.87-dB improvement for 128×128 switch size on average, compared with the average case without optimization. On the other hand, we also investigate the improvement of the highest total crosstalk for a particular traffic matrix (i.e., the worst case of the total crosstalk at output-port that the switching configuration gives the highest total crosstalk at one output-port). In the worst case, the improvement of the total crosstalk at output-port using our optimum scheme is 2.43 dB for 128×128 switch size.

It should be noted that the improvement of total crosstalk for each output is not that significant, compared with that for the total power consumption, the insertion loss

per path as well as the nonuniformity among different output-ports. This is because the optimization of the total crosstalk at each port includes all the possible crosstalk powers from each input-ports, whereas in the previous cases the calculation of the parameters concerned (power consumption, insertion loss, and nonuniformity) for each path does not have contribution from other paths.

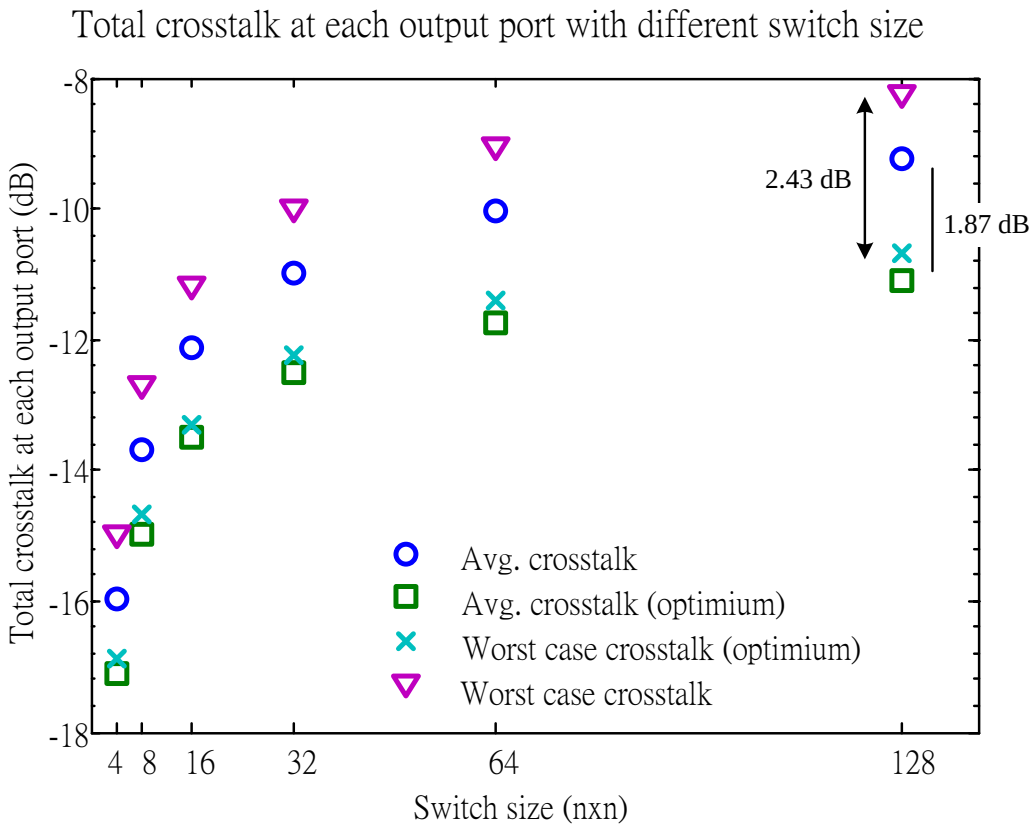


Fig. 4.7. Total crosstalk at each output-port with different switch size

4.4 Summary

In this chapter, we successfully demonstrated that with the optimum switching configuration, the nonuniformity of optical power among different output-ports and the total crosstalk at each output-port can be reduced for microring-based interconnections. We have simulated the results of the nonuniformity of optical power among different output-ports. Results show that in WWCs, with the optimum switching configuration, the best improvement is 9.6 dB, the average improvement is 8.7 dB and the least improvement is 7.2 dB for 128×128 switch size.

On the other hand, for the total cross talk per path, simulation results show that the optimum switching configuration can achieve a 1.87-dB improvement of the total crosstalk at output-port for 128×128 switch size on average, compared with the average case without optimization. Also, the improvement of the total crosstalk at output-port using our optimum scheme is 2.43 dB for 128×128 switch size in the worst case.

Chapter 5

Conclusion and Future Work

5.1 Conclusion of this thesis

In this thesis, we have proposed a generic model, leveraging the asymmetric behaviors of microring switching elements, to optimize the microring-based optical interconnection configurations for the reduction of overall power consumption, total insertion loss per path, non-uniformity and total crosstalk per path. Though microring resonator is a promising candidate in WDM applications like optical interconnections due to its very compact footprint and sub-nanosecond switching time, microring-based optical interconnection has the scalability issue which is limited by the four aforementioned issues including power consumption, insertion loss, nonuniformity and crosstalk.

In Chapter 1, we firstly review the background of microring resonators and microring-based optical interconnections and discuss previous work dedicated to the investigation of asymmetry and scalability issues. Severe asymmetric behaviors that limit the scalability of interconnection are also discussed to give a general background of optical interconnections.

Chapter 2 reviews prior work on the optimization of microring-based interconnection, including the reduction in insertion loss and nonuniformity, which has been discussed in details. The issue of power consumption in optical networks is also discussed and prior work on the reduction of power consumption is reviewed. Besides, we also review the relevant studies on the crosstalk in optical cross-connect networks.

In Chapter 3, we focus on our proposed optimization scheme of microring-based interconnection configurations for the reduction of power consumption and insertion loss. The principle to determine the optimum switching configurations, leveraging the asymmetric behaviors, is illustrated. Calculations of the power consumption and insertion loss in optical interconnections are shown, followed by a novel heuristic.

We successfully demonstrated that with the optimum switching configuration, the overall power consumption and the average total insertion loss per path can be reduced for microring-based interconnections. A new heuristic is also proposed to reduce the computation time for the optimum switching configuration. The results also depict that the optimum average total insertion loss per path using 2B-SEs achieve a 3.65-dB improvement for 128×128 switch size. The optimum average total insertion loss using 2B-SEs in the worst-cast path is shown to be 7.2 dB less than the baseline value without optimization.

Chapter 4 focuses on our proposed optimization scheme of microring-based interconnection configurations for the reduction of nonuniformity and crosstalk. The principle to determine the optimum switching configurations, leveraging the asymmetric behaviors, is illustrated. The calculations of the nonuniformity and crosstalk in optical interconnections are also shown. Finally, simulation results are given and discussed.

We successfully demonstrated that with the optimum switching configuration, the nonuniformity of optical power among different output-ports and the total crosstalk at each output-port can be reduced for microring-based interconnections. We have simulated the results of the nonuniformity of optical power among different output-ports. Results show that in WWCs, with the optimum switching configuration, the best improvement is 9.6 dB, the average improvement is 8.7 dB and the least improvement is 7.2 dB for 128×128 switch size. On the other hand, for the total crosstalk per path, simulation results show that the optimum switching configuration

can achieve a 1.87-dB improvement of the total crosstalk at output-ports for 128×128 switch size on average, compared with the average case without optimization. Also, the improvement of the total crosstalk at output-port using our optimum scheme is 2.43 dB for 128×128 switch size in the worst case.

5.2 Future work

As our proposed scheme leverages on the different behaviors at cross/bar-states for 2B-SEs, those parameters of microrings are critical for optimization of our scheme. It is interesting to design a microring with the optimal parameters such as power consumption, insertion loss and crosstalk for further possible optimizations.

Hence, our future study will focus on the implementation of microring-based interconnections using 2B-SEs with our proposed scheme. It is also worth investigating the possible optimization for other microring-based applications like modulators, filters and multiplexers for a subsystem with a large number of functional devices.

It is interesting to study the joint optimization of the reduction in power consumption, insertion loss, nonuniformity and crosstalk, as the optimum solution for one problem may not be the optimum for other cases. In the joint optimization, we can consider the minimization of the four aforementioned parameters by calculating a single figure of merit, yet to be defined, in order to achieve the global optimum. Another approach for the joint optimization is to prioritize the significance of the four parameters, and then optimize the most important one that satisfies the minimum requirements of the other parameters simultaneously.

List of Publications

[1] Piu-Hung Yuen and Lian-Kuan Chen, "Optimization of Microring-based Optical Interconnection Configurations for the Reduction of Power Consumption and Insertion Loss", *IEEE/OSA Optical Fiber Communication Conference / National Fiber Optic Engineers Conference (OFC/NFOEC)*, paper OW4I.6, 2012.

[2] Piu-Hung Yuen and Lian-Kuan Chen, "Optimization of Microring-based Optical Interconnection Configurations for the Reduction of Power Consumption, Insertion Loss, Nonuniformity and Crosstalk", *IEEE/OSA Journal of Lightwave Technology* (will be submitted in Sept, 2012).

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